INTERBUS-S

User Manual for INTERBUS-S

Slave Protocol Chip SUPI II

IBS SUPI II HB E, Revision : A
Order No.: 27 58 78 7

INTERBUS-S

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Slave Protocol Chip SUPI II

We are constantly attempting to improve the quality of our manuals.

Should you have any suggestions or recommendations for improvement of the contents and organization of our manual, we would appreciate it if you would send your recommendations to:

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1. General

Since 1983 Phoenix Contact took an active part in the fieldbus area and considers the fieldbus as a future-oriented supplement for parallel signal transmission.

However, fieldbus systems are only suitable for industry when the users can go back to their device variety. Therefore, INTERBUS-S has been consistently disclosed from the very beginning to give device manufacturers the possibility of an interface implementation.

In addition to that, protocol chips, such as the IBS SUPI, were developed to keep the expense of interface implementation as low as possbile.

This user manual describes the third generation of INTERBUS slave protocol chips: the IBS SUPI II PLCC and IBS SUPI II QFP.

This user manual forms the basis on which the users can implement their own INTERBUS-S devices, which of course should be subjected to a conformance test in accordance with the end user.

In addition to this user manual we recommend the documentation on the INTERBUS-S conformance test and certification.

INTERBUS-S is a serial sensor/actuator bus. It consists of a central intelligent controller board (controller or IB master) in a host system and distributed I/O modules.

The SUPI II protocol chip is available for the integration of I/O modules in an INTERBUS-S network.

In an INTERBUS-S system, the SUPI II can be implemented in a remote bus station as well as in local bus stations.

On the application side, the SUPI II has a multi-function-pin interface (MFP interface). Corresponding to the functionality of the INTERBUS-S stations, this interface can be configured as a direct I/O interface or as a processor interface.

This user manual contains the information about the SUPI II chip, which is required for the development of your own INTERBUS-S slave station.

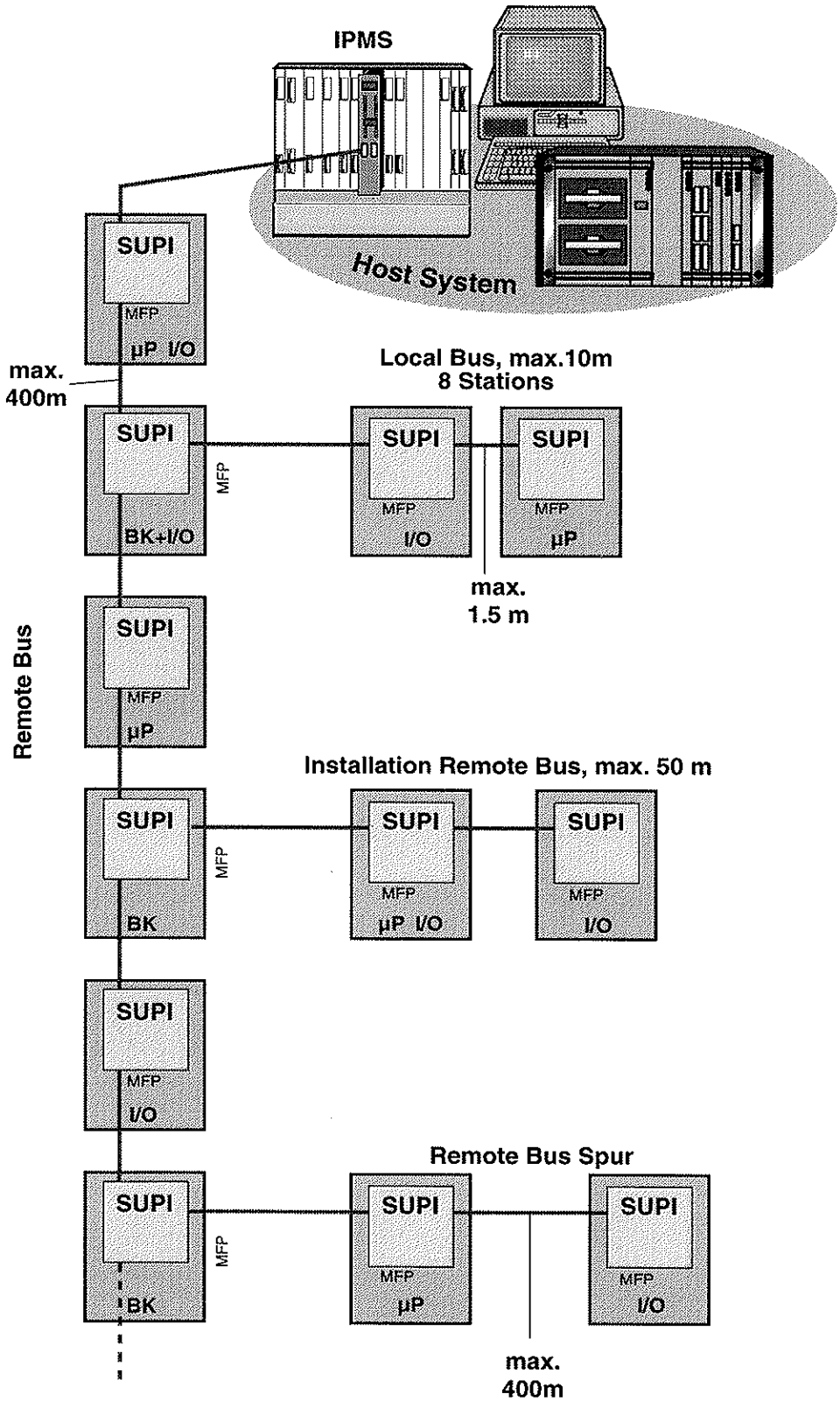


Figure 1-1: Application areas of the INTERBUS-S SUPI II slave protocol chip

2. Introduction

2.1. SUPI II Protocol Chip

The SUPI II protocol chip is an ASIC in 1.0 µm CMOS technology with approx. 7000 gate equivalents and represents the third generation of INTERBUS-S slave components.

The SUPI II is embedded in a PLCC-84 package which is pin-compatible to the SUPI I chip. All operating modes concerning the multi-function interface are compatible in relation to the functions to the SUPI I chip.

Currently, the SUPI II chip is available in two types of packages.

Package	Order designation	Order number
PLCC-84	IBS SUPI II PLCC	27 58 402
QFP-100	IBS SUPI II QFP	27 58 415

2.2. Field of Application

The SUPI II has been designed for industrial applications.

	Value			
Quantity	Min	Type	Max	Unit
Supply voltage	4.5	5.0	5.5	V
Temperature	- 40	+ 25	+ 85	°C

3. Package Types

3.1. PLCC 84 (Plastic Leadless Chip Carrier)

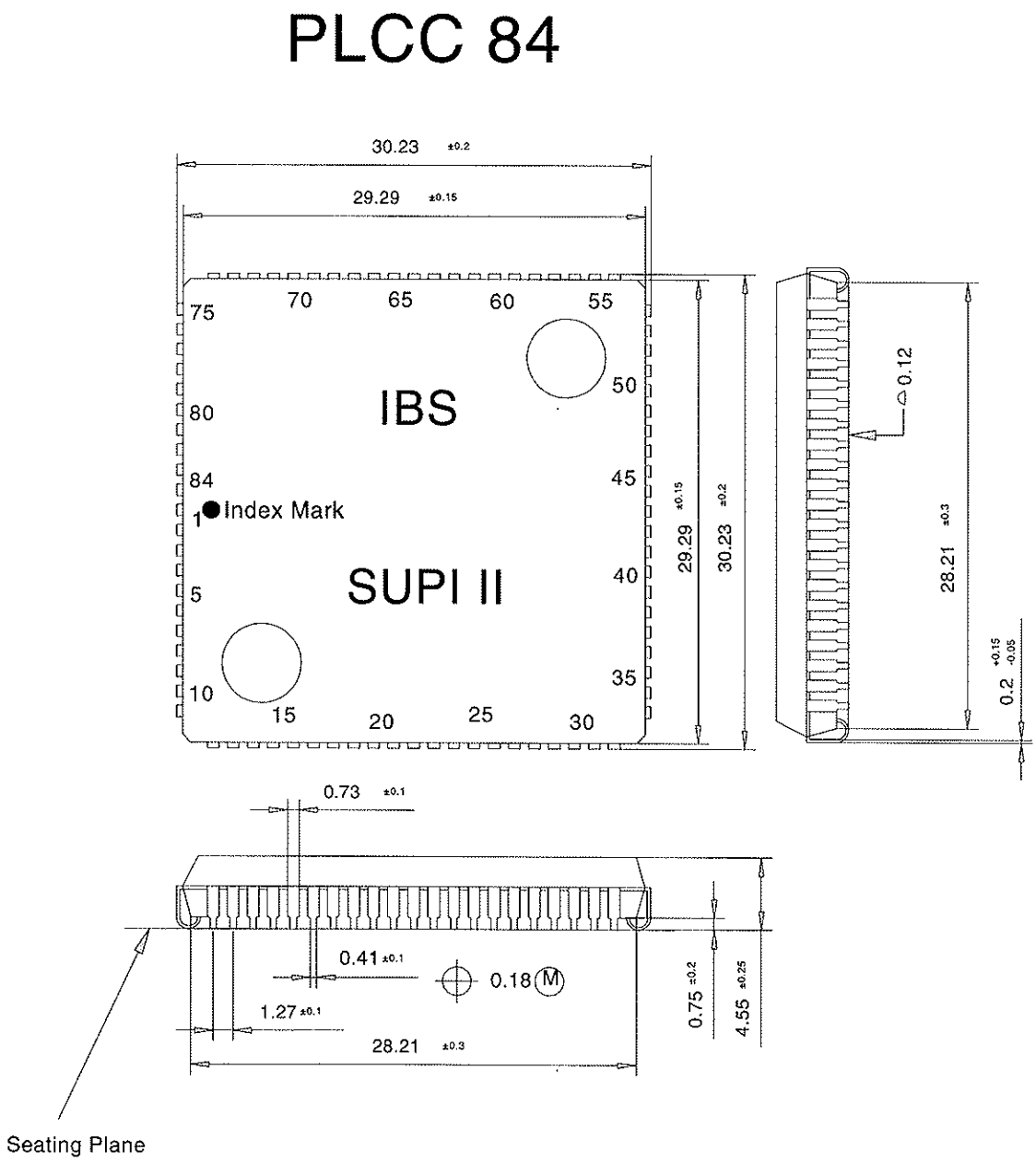


Figure 3-1: PLCC 84 package outline

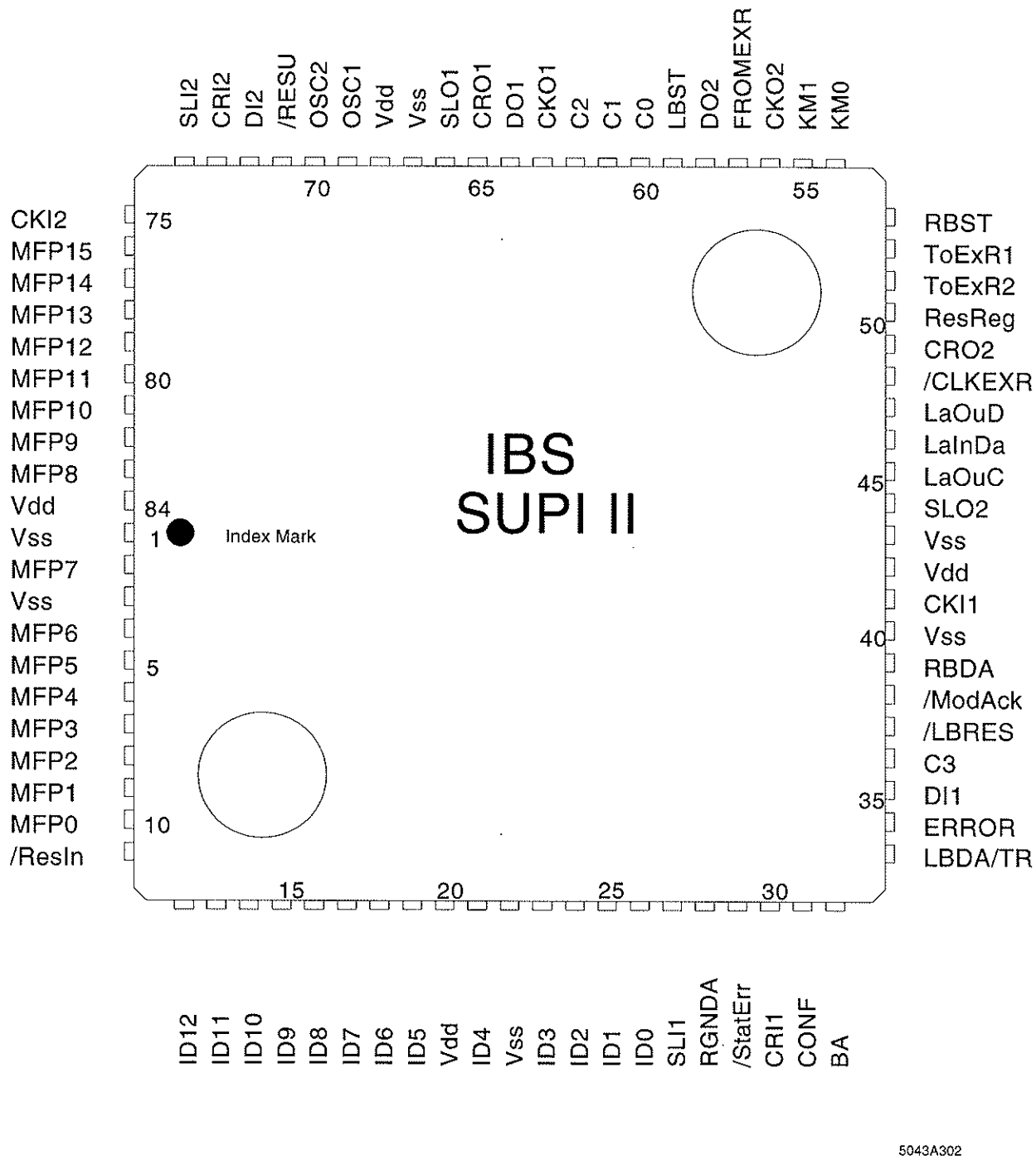


Figure 3-2: Pin layout of the PLCC 84 package

3.2. Pin Assignment of the PLCC 84

Table 3-1: Pin assignment of the PLCC 84

Pin No	Pin Name	Pin No	Pin Name
1	Vss	45	LaOuC
2	MFP7	46	/LaInD
3	Vss.	47	LaOuD
4	MFP6	48	/ClkExR
5	MFP5	49	CRO2
6	MFP4	50	/ResReg
7	MFP3	51	ToExR2
8	MFP2	52	ToExR1
9	MFP1	53	RBST
10	MFP0	54	KM0
11	/ResIn	55	KM1
12	ID12	56	CKO2
13	ID11	57	FromExR
14	ID10	58	DO2
15	ID9	59	LBST
16	ID8	60	C0
17	ID7	61	C1
18	ID6	62	C2
19	ID5	63	CKO1
20	Vdd	64	DO1
21	ID4	65	CRO1
22	Vss	66	SLO1
23	ID3	67	Vss
24	ID2	68	Vdd
25	ID1	69	OSC1
26	ID0	70	OSC2
27	SLI1	71	/ResU
28	RGNDA	72	DI2
29	/StatErr	73	CRI2
30	CRI1	74	SLI2
31	CONF	75	CKI2
32	BA	76	MFP15
33	LBDA/TR	77	MFP14
34	Error	78	MFP13
35	DI1	79	MFP12
36	C3	80	MFP11
37	/LbRes	81	MFP10
38	/ModAck	82	MFP9
39	RBDA	83	MFP8
40	Vss	84	Vdd
41	CKI1		
42	Vdd		
43	Vss		
44	SLO2		

3.3. **QFP 100** (Quad Flat Pack)

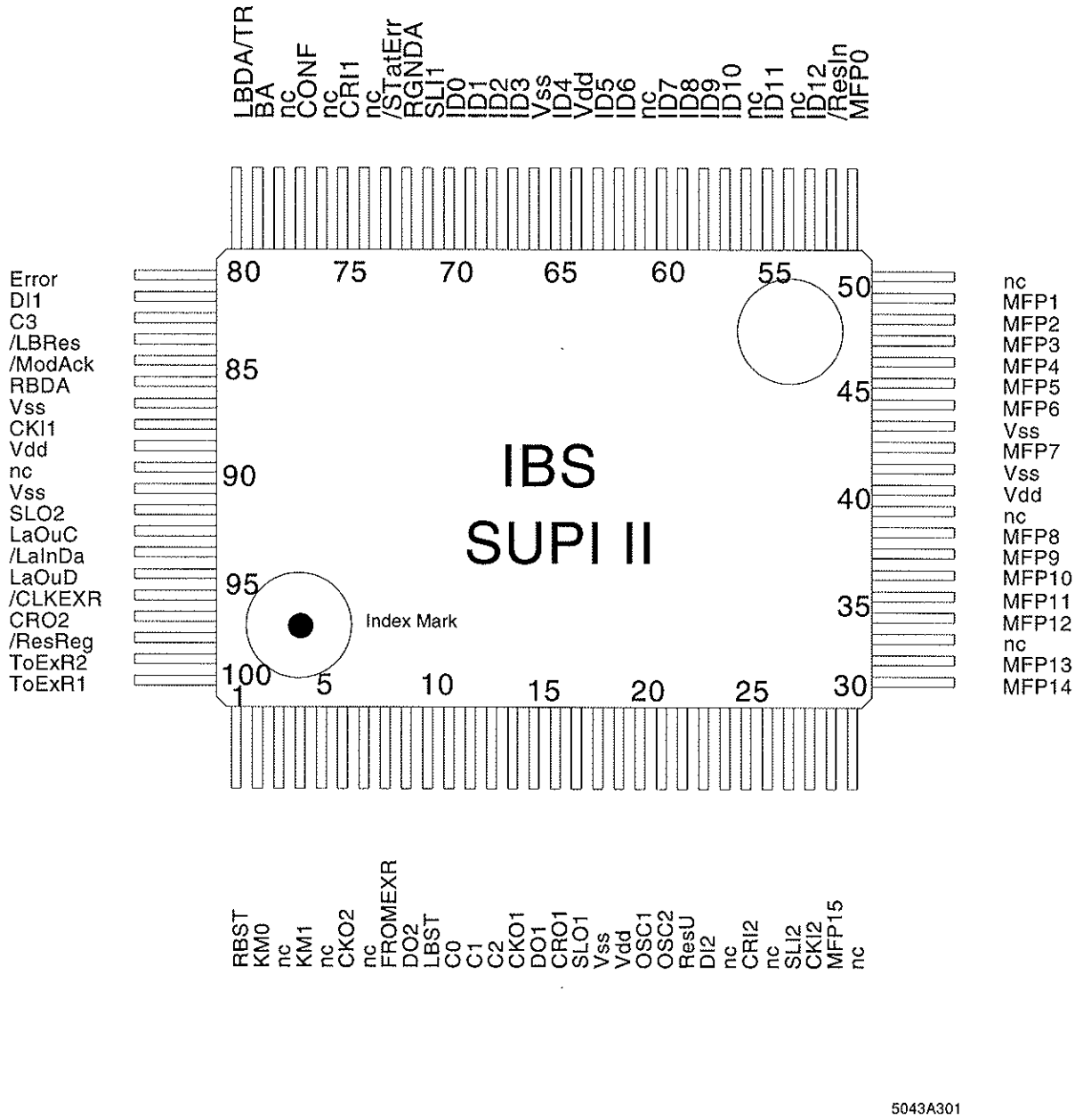


Figure 3-3: Pin layout of the QFP 100 package

3.4. Pin Assignment of the QFP 100

Table 3-2: Pin assignment of the QFP 100

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
1	RBST	45	MFP5	89	Vdd
2	KM0	46	MFP4	90	n.c.
3	n.c.	47	MFP3	91	Vss
4	KM1	48	MFP2	92	SLO2
5	n.c.	49	MFP1	93	LaOuC
6	CKO2	50	n.c.	94	/LaInD
7	n.c.	51	MFP0	95	LaOuD
8	FromExR	52	/ResIn	96	/ClkExR
9	DO2	53	ID12	97	CRO2
10	LBST	54	n.c.	98	/ResReg
11	C0	55	ID11	99	ToExR2
12	C1	56	n.c.	100	ToExR1
13	C2	57	ID10		
14	CKO1	58	ID9		
15	DO1	59	ID8		
16	CRO1	60	ID7		
17	SLO1	61	n.c.		
18	Vss	62	ID6		
19	Vdd	63	ID5		
20	OSC1	64	Vdd		
21	OSC2	65	ID4		
22	/ResU	66	Vss		
23	DI2	67	ID3		
24	n.c.	68	ID2		
25	CRI2	69	ID1		
26	n.c.	70	ID0		
27	SLI2	71	SLI1		
28	CKI2	72	RGNDA		
29	MFP15	73	/StatErr		
30	n.c.	74	n.c.		
31	MFP14	75	CRI1		
32	MFP13	76	n.c.		
33	n.c.	77	CONF		
34	MFP12	78	n.c.		
35	MFP11	79	BA		
36	MFP10	80	LBDA/TR		
37	MFP9	81	Error		
38	MFP8	82	DI1		
39	n.c.	83	C3		
40	Vdd	84	/LbRes		
41	Vss	85	/ModAck		
42	MFP7	86	RBDA		
43	Vss	87	Vss		
44	MFP6	88	CKI1		

n.c. : not connected

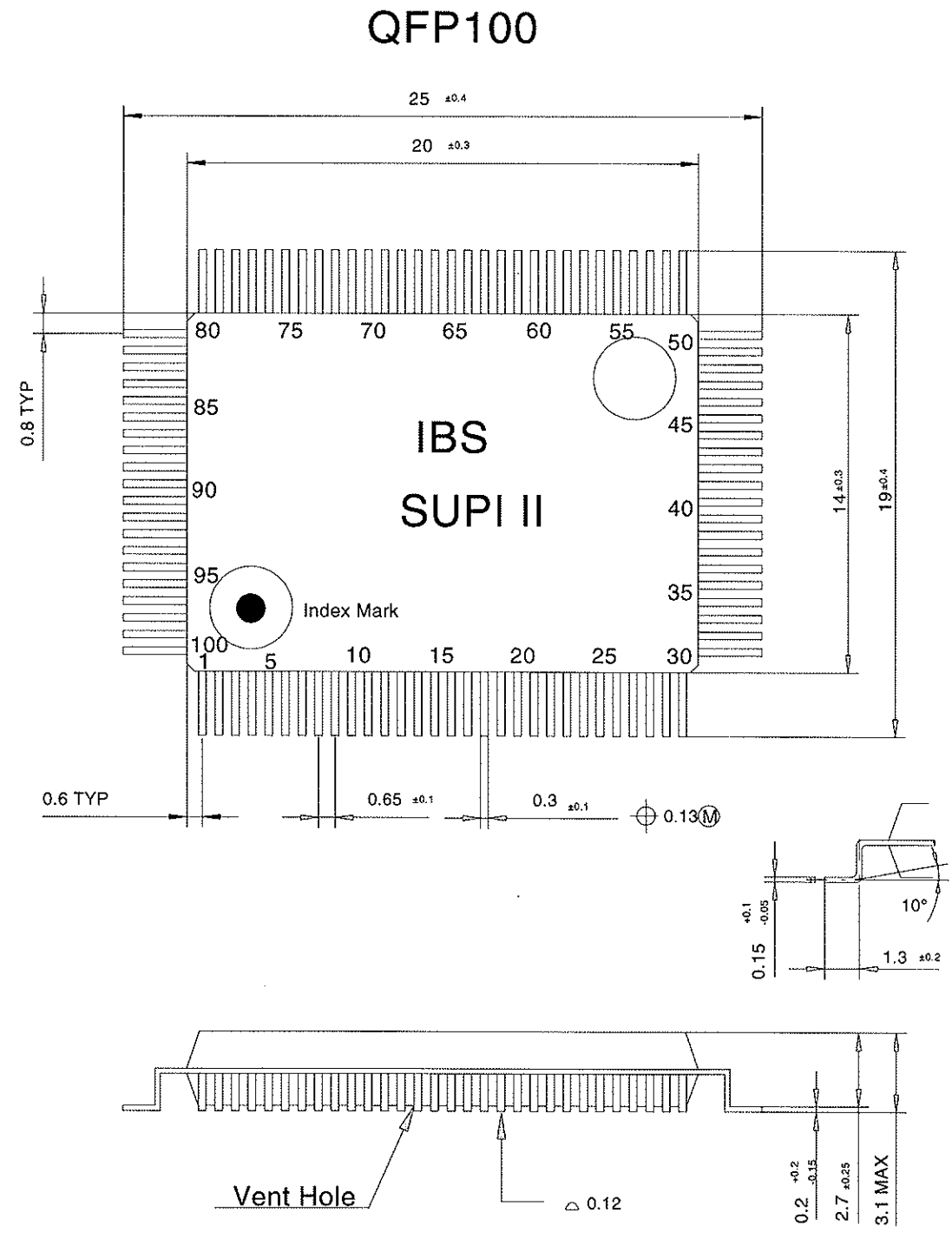


Figure 3-4: QFP 100 package outline

3.5. Pin Description

The listing applies for both package types:

Table 3-3 : Pin description

Mnemonic	Description	Type
OSC1	Oscillator input	OSC
OSC2	Oscillator output	OSC
C3 C2 C1 C0	Configuration inputs for the MFP interface	CI
KM1 KM0 RGNDA	Configuration inputs for the INTERBUS-S interface	CI
ID12- ID0	Identification code setting Data length entry	CI
MFP15- MFP0	Multi-function pins	BD
SLxx	**Control line ID/data cycle**	
SLO1	Select line IN (go path)	ST
SLO2	Select line OUT (go path)	B12
SLI1	Select line OUT (return path)	B12
SLI2	Select line IN (return path)	ST
Dxx	**Data line of the IB-S ring**	
DO1	Data line IN (go path)	ST
DO2	Data line OUT (go path)	B12
DI1	Data line OUT (return path)	B12
DI2	Data line IN (return path)	ST

Mnemonic	Description	Type
CKxx	**Clock line for the IB-S stations**	
CKO1	Clock line IN (go path)	ST
CKO2	Clock line OUT (go path)	B12
CKI1	Clock line OUT (return path)	B12
CKI2	Clock line IN (return path)	ST
CRxx	**Control line check sequence**	
CRO1	Control line IN (go path)	ST
CRO2	Control line OUT (go path)	B12
CRI1	Control line OUT (return path)	B12
CRI2	Control line IN (return path)	ST
/ResIN	INTERBUS reset input	ST
/LBRes	INTERBUS reset output	B2
RBST	Message input whether outgoing InterBus-S interface is used.	CI
LBST	Message input whether local bus interface is used in bus terminal applications. In all other modes of operation this pin is to be connected to V_{dd}.	CI
/StatErr	"Module Error" message input	CI
/ModAck	Acknowledgment ouput for a recognized module error	B2
CONF	"Reconfiguration Request" signal input (for bus terminal modules (BK) only)	CI
RBDA	"Outgoing IB-S Interface" message output is disabled"	B2
LBDA/TR	Message output "Local Bus Disabled" at BK "PCP active" at µP	B2

Mnemonic	Description	Type
BA	"INTERBUS-S active" message output	B2
Error	"Error in the connected local bus" message output for BKs	B2
/CLKExR	Clock for external shift registers	B2
ToExR1	Data output for external shift registers without using the SUPI II-internal shift registers	B2
ToExR2	Data output for external shift registers after use of the SUPI II-internal shift registers	B2
FromExR	Data input for external shift registers	CI
LaOuD	Latch signal of output data Shift registers -> Latch registers	B2
LaOuC	Latch signal of control data Shift registers -> Latch registers	B2
/LaInD	Latch signal of input data Periphery -> Shift registers	B2
/ResReg	Reset signal for external latch registers Can also be used as the "IB-S reset inactive" message output	B2
/ResU	Initialization reset	CI
Vdd	Supply voltage + 5 V	
Vss	Ground	

Explanation of the cell types :

BD : bidirectional, with Schmitt-Trigger inputs and 4 mA driver outputs

CI : CMOS input
ST : Schmitt-Trigger input

B2 : Driver output 2 mA
B12 : Driver output 12 mA

OSC : Oscillator cell

Please refer to Chapter 9 for information about the electrical data.

4. Basic Wiring

4.1 Clock, Initialization

4.1.1 Clock

The SUPI II has an on-chip oscillator. Therefore, for applications in which the 16 MHz clock required by the SUPI II is of no further use, it is sufficient to use a 16 MHz quartz. The quartz is connected to the OSC1 and OSC2 pins. With the two capacitors, that are connected from OSC1 and OSC2 to the ground, the quartz forms a PI circuit. The capacitors have double the value of the load capacitance of the quartz crystal (typ. 68pF with a load capacitance of 30pF). The oscillator cell of the SUPI II also allows to connect capacitors up to 22pF.
In order to set the working point of the on-chip oscillator, a 1MΩ resistor is inserted, from OSC1 to OSC2, parallel to the quartz crystal.
The oscillator can also be operated by an external 16 MHz clock with a CMOS level. In this case, the oscillator operates as a buffer. The external clock signal is to be connected to the OSC1 oscillator input.

Internal oscillator

External clock

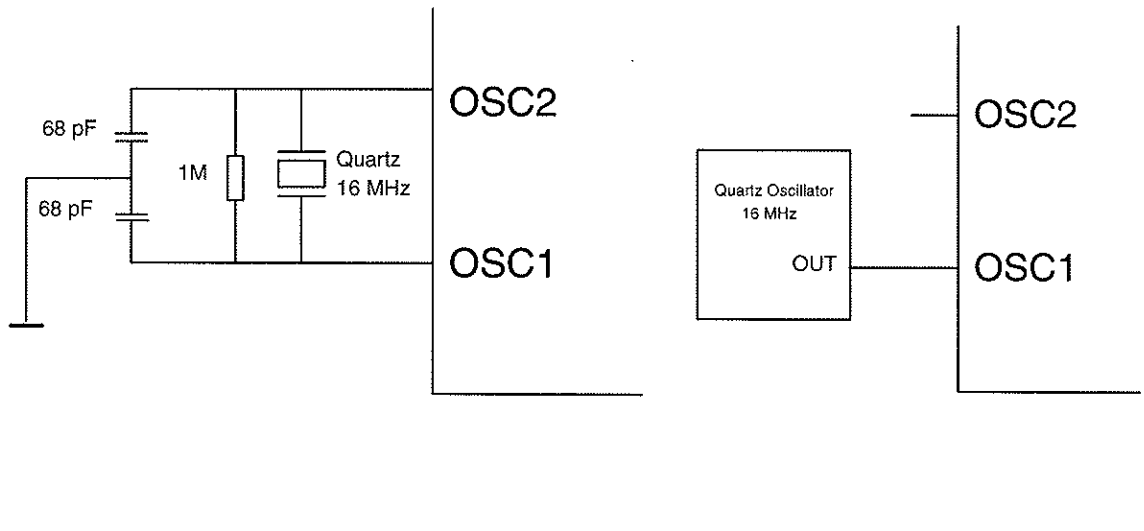


Figure 4-1: Clock lines of the SUPI II

4.1.2 Initialization

In order to put the SUPI II chip to a defined state after power-on, it is necessary to keep the /ResU initialization input to "low" during the power-on phase. During operation the /ResU is to be set to "high".

4.2 Configuration Options

4.2.1 INTERBUS-S Interfaces

The SUPI II has two separate INTERBUS-S interfaces, and one interface to the application.

The SUPI II can be interfaced to the INTERBUS-S remote bus or local bus.

The RGNDA pin of the SUPI II determines whether the chip will be used for a remote or local bus station.

In addition, pins KM0, KM1, and CK01 have to be configured according to the following table:

KM0	KM1	CKO1	RgnDA	IB-S interface mode
0	0	-	1	Local bus, 8-wire
1	1	0	0	Remote bus, 2-wire 500 kbits

For 8-wire applications, pin CKO1 is the incoming INTERBUS-S clock line.

4.2.2 Multi-Function-Pin Interface

The 16-bit wide multi-function pin interface (short: MFP) is available as the interface to the application.

The configuration pins C3, C2, C1, C0 allow the following interface connections to the INTERBUS-S network:

Table 4-1: Configuration of the MFP interface

C3	C2	C1	C0	MFP mode
1	0	0	0	Bus terminal mod. 8-wire local bus
0	0	1	1	Bus terminal mod. I/O with 8-wire local bus
0	0	0	0	Bus terminal mod. 2-wire spur line
0	1	0	0	Bus terminal mod. I/O with 2-wire spur line
1	0	0	1	16-bit output
1	0	1	0	16-bit input
1	1	0	1	8-bit input and 8-bit output
0	0	0	1	µP interface, 1 byte
1	0	1	1	µP interface, 2 bytes
1	1	1	1	µP interface, 4 bytes
1	1	0	0	µP interface, 6 bytes
0	0	1	0	µP interface, 8 bytes

4.2.3 Identification Code

Each INTERBUS-S station has an identification code which can be read by the INTERBUS-S master (controller) in an identification cycle (ID cycle).
The INTERBUS-S master obtains information from the identification code about the type of station and its data register length in a data cycle.
The identification code consists of 3 groups. An 8-bit code is applied to the pins ID0 - ID7. The INTERBUS-S Club has determined this code in the "INTERBUS-S Specification - Identification Codes", depending on the respective functionality of the station.
Pins ID8 - ID12 specify the data width of the bus station. It is to be set for each station according to the following table :

Table 4-2 : ID code data width

ID12	ID11	ID10	ID9	ID8	Data width	
0	0	0	0	0	0 Words	
0	0	0	0	1	1 Word	
0	0	0	1	0	2 Words	
0	0	0	1	1	3 Words	
0	0	1	0	0	4 Words	
0	0	1	0	1	5 Words	
0	0	1	1	0	8 Words	
0	0	1	1	1	9 Words	
0	1	0	0	0	1 Nibble	**
0	1	0	0	1	1 Byte	**
0	1	0	1	0	3 Nibbles	**
0	1	0	1	1	3 Bytes	**
0	1	1	0	0	5 Nibbles	**
0	1	1	0	1	5 Bytes	**
0	1	1	1	0	6 Words	*
0	1	1	1	1	7 Words	*
1	0	0	1	0	16 Words	*
1	0	0	1	1	24 Words	*
1	0	1	0	0	32 Words	*
1	0	1	0	1	10 Words	*
1	0	1	1	0	12 Words	*
1	0	1	1	1	14 Words	*

* This data width will only be supported as of firmware version 3.20 by the controller boards and as of version 2.0 by the PC AT board.
** This data width is currently not yet supported.

5. InterBus-S Interfaces

5.1 Overview

When the chip is interfaced to INTERBUS-S, it can be embedded in a remote bus or local bus station.

The remote bus station is always chosen when large distances (cable connections up to 400 m) have to be covered, or if the number of signal lines is to be as small as possible.
An asynchronous 2-wire protocol and a differential voltage interface according to RS-422 are used in the remote bus.
Therefore, the bus cable requires 5 signal lines.

The 2-wire protocol is simply another kind of physical transmission of the 8-wire protocol, i.e. all protection and check mechanisms of the 8-wire protocol are also effective for the 2-wire protocol.

A remote bus station always has its own voltage supply.
In the case of a remote bus failure, the entire network can only be operated up to the last functioning remote bus station. Post-connected modules cannot be addressed anymore.

A local bus station is used where the physical distance to the next module is limited to less than 10 m (e.g. switch cabinet level).

The synchronous 8-wire protocol which CMOS levels is used for the local bus.
The entire logic required for the INTERBUS-S interface is supplied by the pre-connected bus terminal module through a supply line in the bus cable. This allows to operate the INTERBUS-S interface even if the application voltage fails.

When a local bus station fails, the bus terminal module can isolate the defective local bus from the network. This allows to continue operation of the rest of the network.

5.2 Local Bus Connection

KM0	KM1	CKO1	RgnDA	IB-S interface mode
0	0	-	1	Local bus, 8-wire

The RGNDA pin is to be set to high and the KM0 and KM1 pins to low for local bus applications.
The bus signal pins of the SUPI II fulfill the INTERBUS-S specifications of the local bus.
The 9 V- supply to the local bus is to be lowered to 5 V and to be monitored.
The active low output signal of the monitoring module is connected to the /RESU initialization input.
The RBST pin is connected with pin 4 of the local bus output connector. Without an output connector (RBST=0), the outgoing interface is switched off and diverted to the return path by the circuitries inside the chip.

The following two applications show local bus interfaces with and without electrical isolation. Please pay attention to the fact that for 'local bus with electrical isolation' applications the INTERBUS-S logic and, therefore, the entire local bus cannot be operated any longer after a failure of the application voltage.

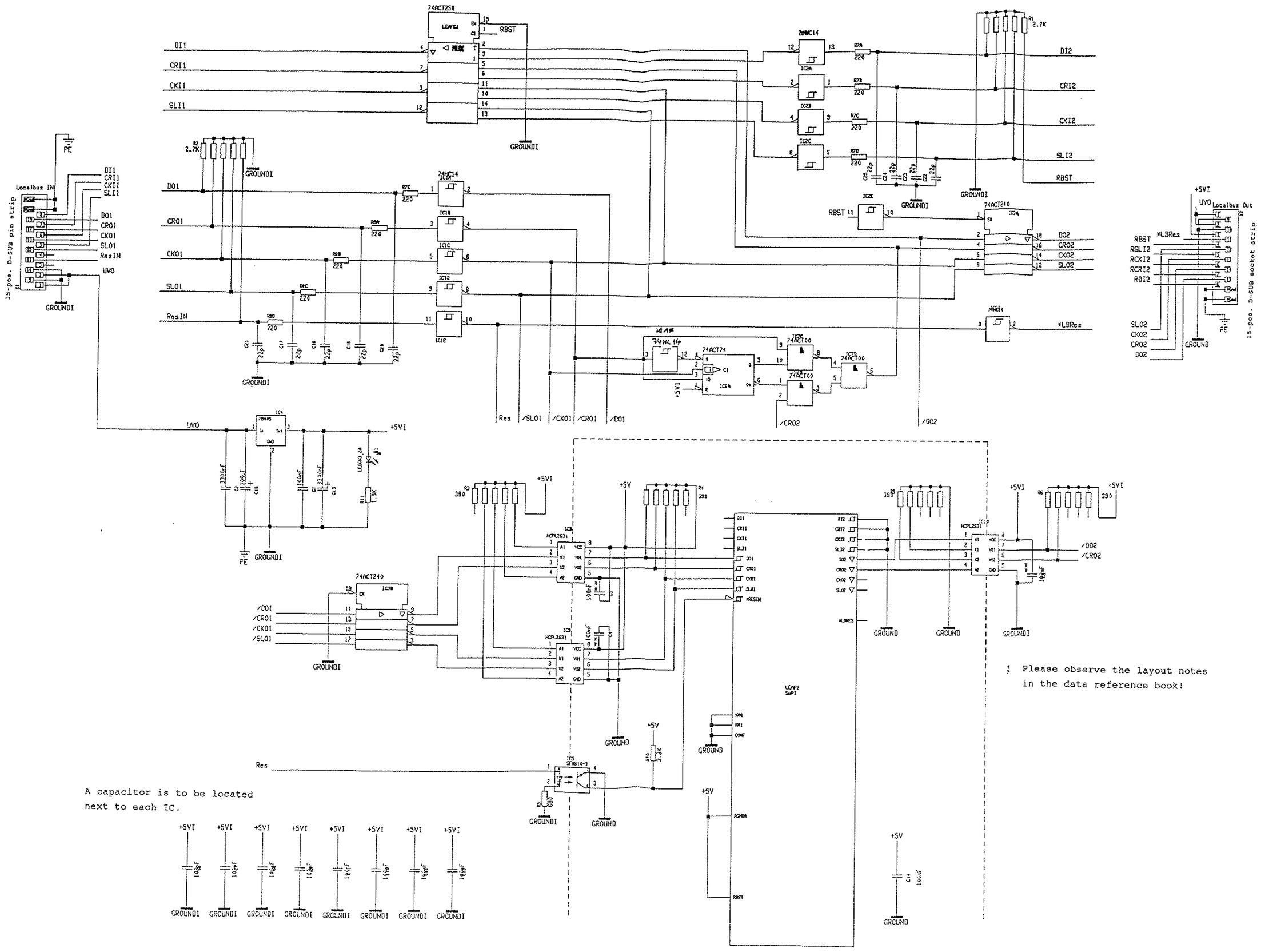
15-pos. D-SUB connectors are used for the local bus.
The following tabe lists the assignments of the input and output interfaces.

Table 5-1 : Pin assignment of a 15-pos. D-SUB local bus interface connector

Pin No.	Signal name of the incoming interface (male conn.)	Signal name of the outgoing interface (female conn.)
1	+ 9 V	+ 9 V
2	+ 9 V	+ 9 V
3	unused	+ 5 V
4	unused	RBST
5	SLI1	SLI2
6	CKI1	CKI2
7	CRI1	CRI2
8	DI1	DI2
9	GND	GND
10	GND	GND
11	/ResIn	/LBRes
12	SLO1	SLO2
13	CKO1	CKO2
14	CRO1	CRO2
15	DO1	DO2

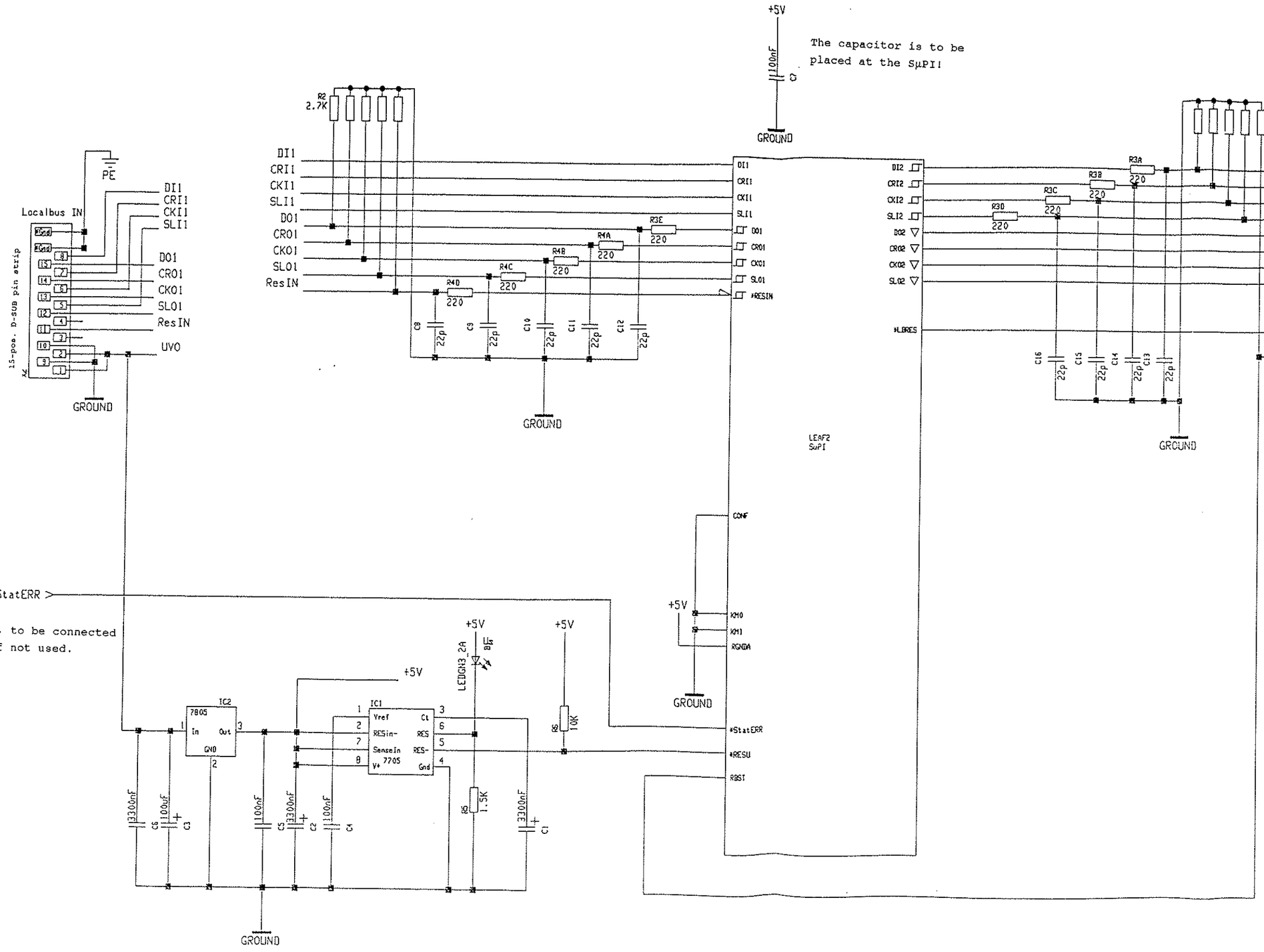
Applikation : Peripheriebusankopplung mit galv. Trennung

(Application: Local bus with electrical isolation)



Applikation : Peripheriebusankopplung

(Application: Local bus without electrical isolation)



5.3 Remote Bus Connection

KM0	KM1	CKO1	RgnDA	IB-S interface mode
1	1	0	0	Remote bus; 2-wire, 500 kbits

RS-485 drivers and receivers are pre-connected to the INTERBUS-S interface. The two INTERBUS-S interfaces only consist of the DO1, DI1, DO2, and DI2 data lines. All other input signals of the two interfaces are to be connected to a defined potential (low or high). The incoming remote bus interface can be provided with optocouplers for electrical isolation. The RBST is connected to pin 9 of the remote bus output connector. Without an output connector (RBST=0), the outgoing interface is switched off and is diverted to the return path by the circuitries inside the chip.

By default, 9-pos. D-SUB connectors are used in the remote bus.
The following table lists the assignment of the input and output interfaces.

Table 5-2: Pin assignment of a 9-pos. D-SUB remote bus interface connector

Pin No.	Signal name of the incoming interface (male conn.)	Signal name of the outgoing interface (female conn.)
1	DO1	DO2
2	DI1	DI2
3	GND	GND
4	unused	unused
5	unused	+ 5V
6	/DO1	/DO2
7	/DI1	/DI2
8	unused	unused
9	unused	RBST

Applikation : 2-Leiter Fernbusankopplung mit galv. Trennung

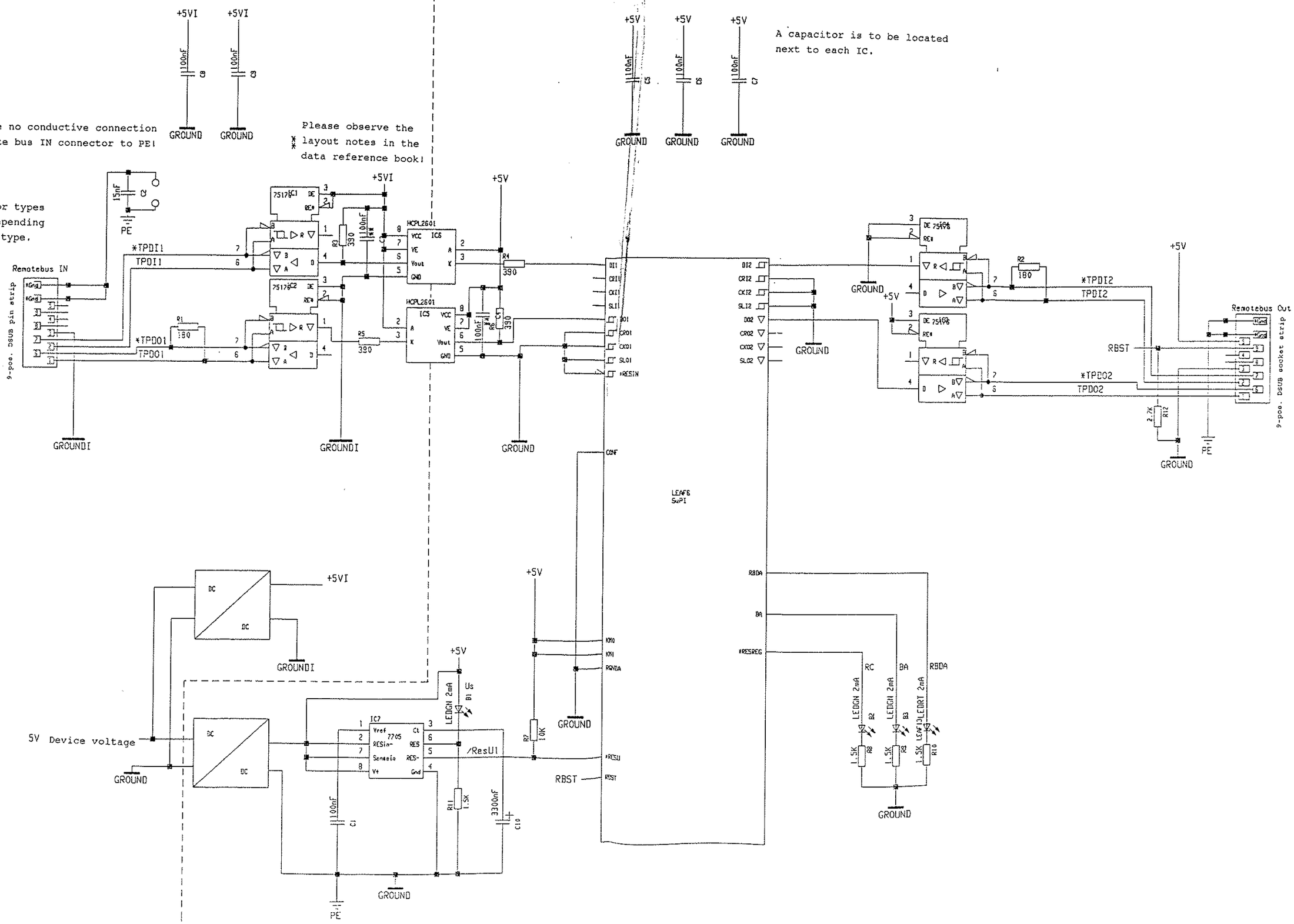
(Application: 2-wire remote bus with electrical isolation)

There shall be no conductive connection from the remote bus IN connector to PE!

* Other connector types may be used depending on the device type.

** Please observe the layout notes in the data reference book!

A capacitor is to be located next to each IC.



6. MFP Interfaces

6.1 Overview

The configuration of the MFP interface determines how the application accesses the INTERBUS-S interface via the SUPI II chip.

The following three classes will be distinguished:

- Bus terminals modules,

- Direct input/output

- Access with the help of a microprocessor (µP interface)

The following table shows the three classes and the configuration via the pins C3, C2, C1 and C0.

Table 6-1 : Operating modes of the MFP interface

C3	C2	C1	C0	MFP mode
1	0	0	0	BK, 8-wire local bus
0	0	1	1	BK, I/O with 8-wire local bus
0	0	0	0	BK, 2-wire spure line
0	1	0	0	BK, I/O with 2-wire spur line
1	0	0	1	16-bit output
1	0	1	0	16-bit input
1	1	0	1	8-bit input and 8-bit output
0	0	0	1	µP interface, 1 byte
1	0	1	1	µP interface, 2 bytes
1	1	1	1	µP interface, 4 bytes
1	1	0	0	µP interface, 6 bytes
0	0	1	0	µP interface, 8 bytes

6.2 Bus Terminal Module Mode

A bus terminal module (BK) connects the INTERBUS-S local bus stations installed in the field with the INTERBUS-S remote bus.
The BK also makes available the voltage supply (9V/1A) for the INTERBUS-S logic of the local bus stations.
In addition, the BK - on request of the INTERBUS-S master - can connect or disconnect the connected local bus to or from the rest of the network.

C3	C2	C1	C0	MFP mode
1	0	0	0	BK, 8-wire local bus
0	0	1	1	BK, I/O with 8-wire local bus

A distinction is made between a standard bus terminal module (BK) and a bus terminal module with I/O points (BK I/O).

The standard bus terminal function fulfills the functions described above.
It does not have its own I/O points so that a data width of 0 is internally set.
Since no external I/O points can be implemented, the FromExR input pin is to be set to a low level.

In addition to the BK functions described above, the bus terminal modules with I/O points can loop in external I/O points between pins ToExR1 and FromExR. If no external I/O points are implemented, pins ToExR1 and FromExR have to be bridged for this mode of operation.

(see also Chapter "Register Expansion")

Both modes of operation provide an 8-wire interface as local bus, which is made available at the MFP interface according to the following table.

Tabe 6-2: Assignment of the MFP interface for the BK mode

MFP(n)	Assignment	
0	CKI	Clock line input
1	SLI	Control line data/ID cycle input
2	DI	Data line input
3	CRI	Control line check sequence input
4	CKO	Clock line output
5	SLO	Control line data/ID cycle output
6	DO	Data line output
7	CRO	Control line check sequence output
8	ALARM	Alarm output*
9	X	
10	X	
11	X	
12	X	
13	X	
14	X	
15	X	

X : not to be used
* The INTERBUS-S master can set the alarm output.

In this case the /LBRes reset signal belongs to the complete 8-wire local bus interface. In these modes, the LBST message input is also used to recognize a plugged local bus cable.

A second group within the "bus terminal module" class are BKs which 2-wire spurs as an additional INTERBUS-S interface. The 2-wire spur can be used for setting up an installation remote bus segment.
In this group a distinction is also made between a BK and a BK I/O.

C3	C2	C1	C0	MFP mode
0	0	0	0	BK, 2-wire spur line
0	1	0	0	BK, I/O with 2-wire spur line

In this group, the MFP interface has the following assignment.

Table 6-3: Assignment of the MFP interface for the BK with 2-wire-spur mode

MFP(n)	Assignment	
0	X	
1	X	
2	DI	Data line input
3	X	
4	X	
5	X	
6	DO	Data line output
7	X	
8	ALARM	Alarm output *
9	X	
10	X	
11	X	
12	X	
13	X	
14	X	
15	X	

X : not to be used
* The INTERBUS-S master can set the alarm output.

In these modes, the LBST message input is used to recognize a connected local bus station.

6.3 I/O Mode

6.3.1 16-Bit Output

In the 16-bit output mode, the INTERBUS OUT data of the first two internal OUT registers are available in parallel at the multi-function pins and can be connected directly to the application.
The data is updated synchronous to the INTERBUS-S cycle.
For the outputs, 4 mA CMOS drivers are used.
If no additional I/O points are to be used, then the ToExR2 and FromExR pins are to be connected together.
Should additional IN data be used, then external shift registers are to be connected between the ToExR1 and FromExR pins. The OUT data can be expanded by the connection of external shift registers to the ToExR2 pin (see also Chapter "Register Expansion").

C3	C2	C1	C0	MFP mode
1	0	0	1	16-bit output

In this mode the MFP interface has the following assignment

Table 6-4: Assignment of the MFP interface for the 16-bit output mode

MFP(n)	Assignment	Significance
0	By0A(0)	2^8
1	By0A(1)	2^9
2	By0A(2)	2^{10}
3	By0A(3)	2^{11}
4	By0A(4)	2^{12}
5	By0A(5)	2^{13}
6	By0A(6)	2^{14}
7	By0A(7)	2^{15} MSB
8	By1A(0)	2^0 LSB
9	By1A(1)	2^1
10	By1A(2)	2^2
11	By1A(3)	2^3
12	By1A(4)	2^4
13	By1A(5)	2^5
14	By1A(6)	2^6
15	By1A(7)	2^7

6.3.2 16-Bit Input

In the 16-bit input mode of operation, the application can lead 16 parallel signals directly to the multi-function pins. The inputs are laid out as CMOS Schmitt-Trigger. The data is taken over synchronous to the INTERBUS-S cycle and transferred to the INTERBUS-S master.
The data width can be expanded by external shift registers, which are connected between ToExR2 and FromExR. Should additional OUT data be used, then these shift registers are to be connected to the ToExR1 pin.
If no external expansion is required, then the ToExR2 and FROMEXR pins are to be connected together.

C3	C2	C1	C0	MFP mode
1	0	1	0	16-bit input

In this mode the MFP interface has the following assignment.

Table 6-5: Assignment of the MFP interface for the 16-bit input mode

MFP(n)	Assignment	Significance
0	By0E(0)	2^8
1	By0E(1)	2^9
2	By0E(2)	2^{10}
3	By0E(3)	2^{11}
4	By0E(4)	2^{12}
5	By0E(5)	2^{13}
6	By0E(6)	2^{14}
7	By0E(7)	2^{15} MSB
8	By1E(0)	2^0 LSB
9	By1E(1)	2^1
10	By1E(2)	2^2
11	By1E(3)	2^3
12	By1E(4)	2^4
13	By1E(5)	2^5
14	By1E(6)	2^6
15	By1E(7)	2^7

6.3.3 8-Bit Input and 8-Bit Output

Unlike the two I/O modes described above, this mode does not represent a 16-bit but an 8-bit station.
The MFP interface is configured in such a way that both the 8-bit input as well as the 8-bit output is possible simultaneously without register expansion.

You have to observe (see also Chapter "Idenfication Code") that the INTERBUS-S master controller board currently not yet supports the data width of 1 byte (8 bits).

If this mode is required, the station width must be extended to 16 bits with an external 8-bit shift register.

C3	C2	C1	C0	MFP mode
1	1	0	1	8-bit input and 8-bit output

In this mode the MFP interface has the following assignment.

Table 6-6: Assignment of the MFP interface for the 8-bit input and 8 output mode

MFP(n)	Assignment	Significance	
0	By0A(0)	2^0 LSB	Output byte
1	By0A(1)	2^1	
2	By0A(2)	2^2	
3	By0A(3)	2^3	
4	By0A(4)	2^4	
5	By0A(5)	2^5	
6	By0A(6)	2^6	
7	By0A(7)	2^7 MSB	
8	By0E(0)	2^0 LSB	Input byte
9	By0E(1)	2^1	
10	By0E(2)	2^2	
11	By0E(3)	2^3	
12	By0E(4)	2^4	
13	By0E(5)	2^5	
14	By0E(6)	2^6	
15	By0E(7)	2^7 MSB	

6.4 µP Access Mode

In the µP access mode it is possible to address the SUPI II chip from a microprocessor, like a peripheral component (e.g. RAM).
For this purpose, the SUPI II has an 8-bit wide, bidirectional data bus D(7:0), a 4-bit address bus A(3:0), the active low control signals chip-select /CS, read /RD and write /WR, as well as an active-low interrupt request line/IRQ.

The MFP interface has the following assignment:

Table 6-7: Assignment of the MFP interface for the µP access mode

MFP(n)	Assignment
0	A0
1	A1
2	A2
3	A3
4	/RD
5	/WR
6	/CS
7	/IRQ
8	D0
9	D1
10	D2
11	D3
12	D4
13	D5
14	D6
15	D7

6.4.1 MFP Interface Timing

Write access

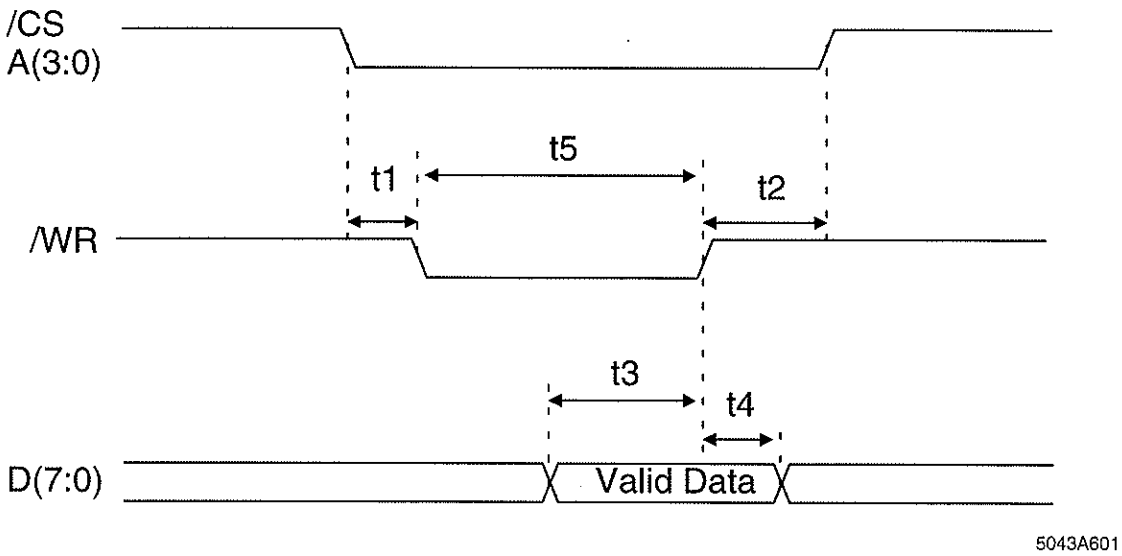


Figure 6-1: Timing of the MFP interface - write access

Table 6-8: Timing of the MFP interface - write access

Symbol	Meaning	Time/ns min.
t1	Addresses and /CS valid before negative edge /WR	5
t2	Addresses and /CS valid after positive edge /WR	5
t3	Valid data before positive edge /WR	15
t4	Valid data after positive edge /WR	10
t5	/WR pulse width	30

Read access

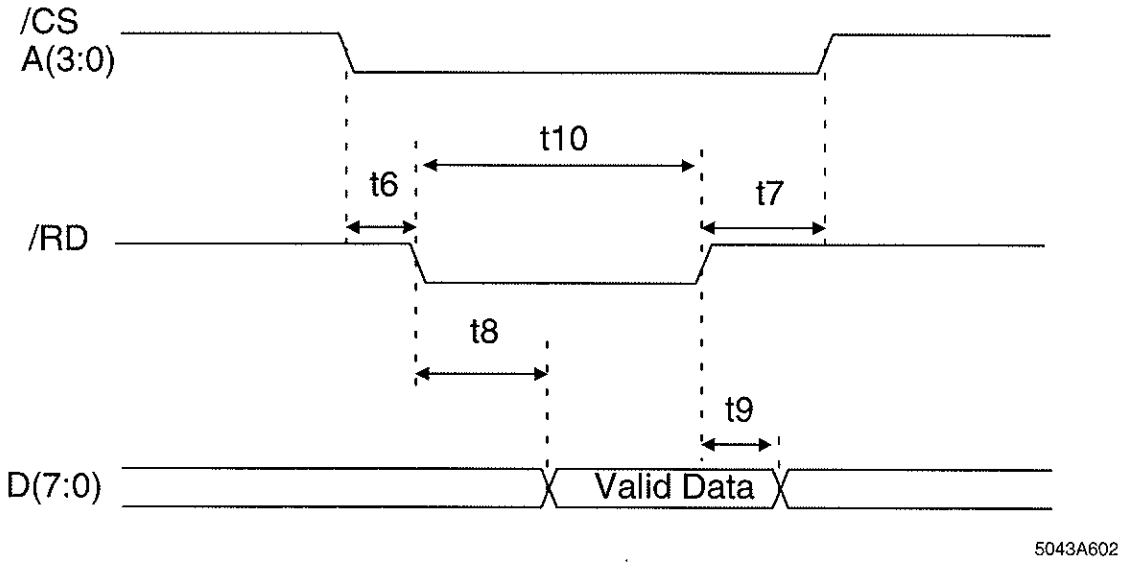


Figure 6-2: Timing of the MFP interface - read access

Table 6-9 : Timing of the MFP interface - read access

Symbol	Meaning	Time/ns min.	max.
t6	Addresses and /CS stable before neg. edge of /RD	10	
t7	Addresses and /CS stable after pos. edge of /RD	10	
t8	Valid data after negative edge of /RD		25
t9	Data bus high-resistance after pos. edge /RD		25
t10	/RD pulse width	30	

6.4.2 µP Modes of Operation

Table 6-10: µP modes of operation

SUPI Pin				
C3	**C2**	**C1**	**C0**	**MFP interface mode**
0	0	0	1	µP interface, 1 byte
1	0	1	1	µP interface, 2 bytes
1	1	1	1	µP interface, 4 bytes
1	1	0	0	µP interface, 6 bytes
0	0	1	0	µP interface, 8 bytes

In the µP modes of operation, the data width may vary between one and eight bytes.
The five µP modes, therefore, differ only with respect to the active data width. This data width can also be changed with the software (see Chapter "SET II-Register").

The following descriptions of the registers are independent of the selected µP mode.

6.4.3 Address Area Assignment

The SUPI II provides four address lines, A3 -A0.
The address area assignment is backward-compatible to the SUPI I chip.

Table 6-11: Address area assignment of the SUPI II chip

Rel. address	Write register	Read register
0	IB-IN Byte 0	IB-OUT Byte 0
1	IB-IN Byte 1	IB-OUT Byte 1
2	IB-IN Byte 2	IB-OUT Byte 2
3	IB-IN Byte 3	IB-OUT Byte 3
4	Interrupt Enable	Interrupt Event I
5	Set I	Interrupt Event II
6	Set II	Test State
7	Unused	IB-State
8	Cycle Write	Cycle Read
9	Test Mode	Unused
10	IB-IN Byte 4	IB OUT Byte 4
11	IB-IN Byte 5	IB OUT Byte 5
12	IB-IN Byte 6	IB OUT Byte 6
13	IB-IN Byte 7	IB OUT Byte 7

All registers of the SUPI II chip have the default value 0.

6.4.4 INTERBUS-S Data Registers

The INTERBUS-S data registers with the addresses 0-3 and 10-13 are intended for the exchange of the I/O data between the application and the INTERBUS-S master.
The data registers designated IB-IN byte are to be written by the application, while the IB-OUT byte data registers are to be read by the application.

Please consider that the IB-IN bytes 0 and 1 are cleared automatically after data is transferred over the bus (default setting).

If this data register is not cyclically written to, the written data item will consequently be sent only once. Afterwards, the value 0 is transferred in those bytes.

For applications in which no PCP communication is used, the value 04hex is to be written once in the SET-I register with the relative address 5 after initialization has been completed. In doing so, the automatic clearing of the IB-IN bytes 0 and 1 is deactivated.

The significance of the data registers decreases with the addresses increasing, i.e. for a station with a data width of 8 bytes, the byte with address 0 is the most significant byte, the byte with the address 13 the least significant byte.

6.4.5 Interrupt Mode

Since the connected microprocessor typically writes and reads the data registers asynchronously to the INTERBUS-S cycle, inconsistent data may occur, when the reading and writing coincides with the latch phase* of an INTERBUS-S cycle.

For this purpose, the SUPI II chip has an interrupt logic, which makes available several INTERBUS-S-cycle-synchronous events as interrupts.

In addition, it is also possible to use certain events as polling bits.

The different interrupt sources are enabled via a common interrupt enable register by setting the corresponding bit to the value "1".
After an interrupt event (/IRQ becomes 0) occurs, the source can either be read in the interrupt event I register and/or in the interrupt event-II register. The bit which corresponds to the event is set to "1".

The read access causes an automatic reset of the registers and the /IRQ request line.

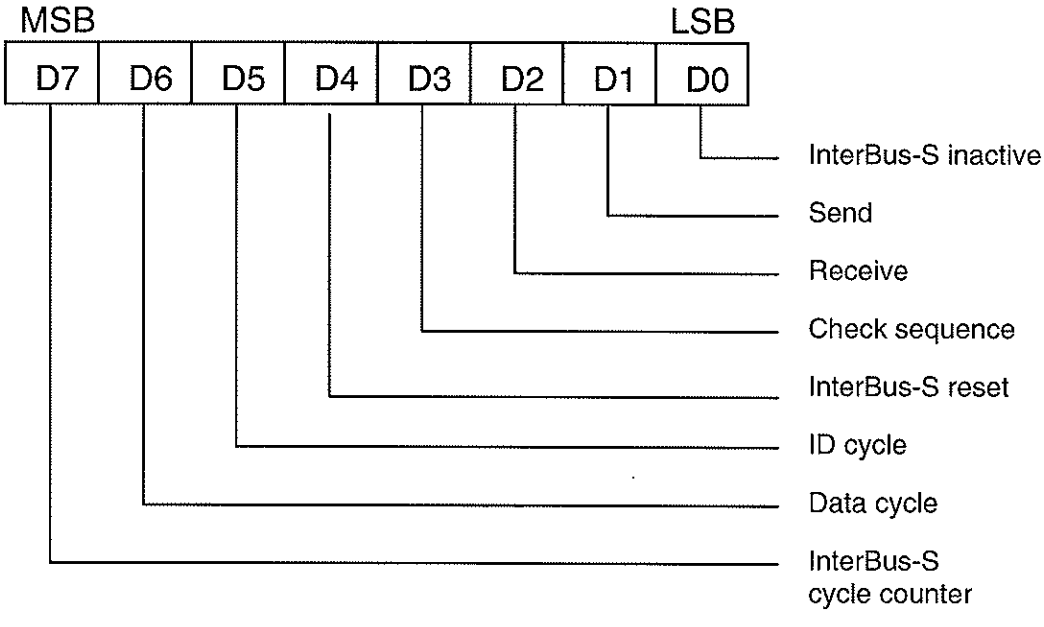
* The latch phase completes the check sequence of each INTERBUS-S cycle. In this latch phase, secured OUT data is stored in the IB-OUT data registers and data is transferred from the IB-IN data registers to INTERBUS-S.

6.4.6 Interrupt Enable Register

Relative **write address : 4**

The interrupt-enable register allows to enable the interrupt sources of the interrupt-event-I registers and interrupt-event-II registers separately.

Assignment:



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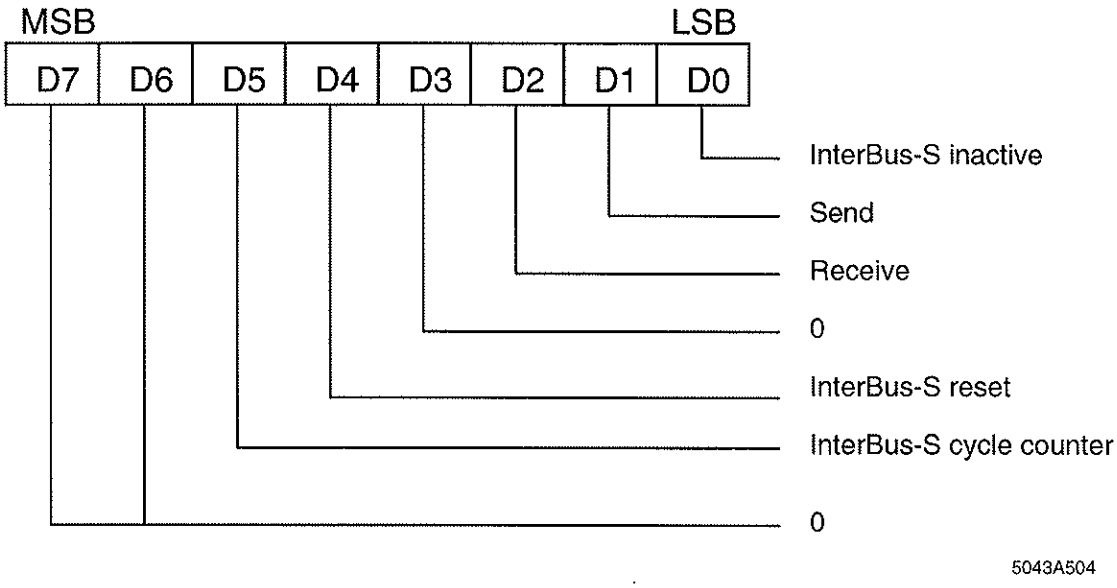
6.4.7 Interrupt-Event-I Register

Relative **read address : 4**

Assignment:

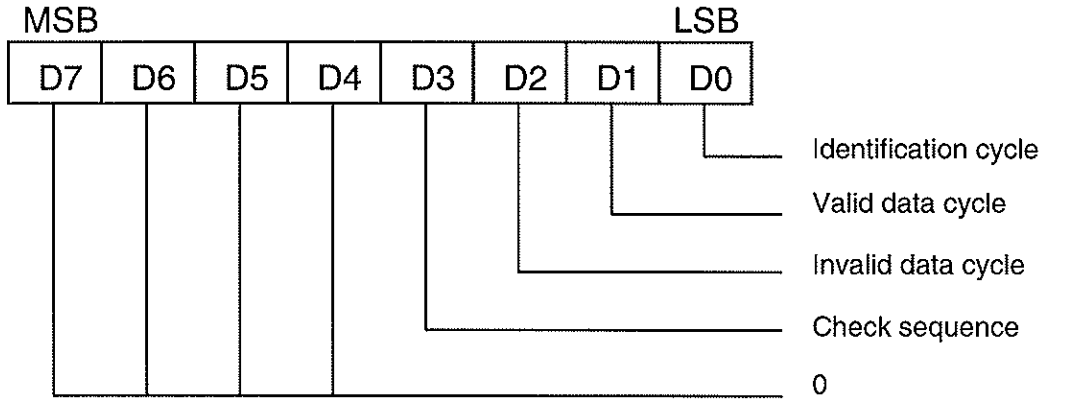


6.4.8 Interrupt-Event-II Register

Relative **read address : 5**

The remaining INTERBUS-S events are stored in this register.

Assignment:



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6.4.8.1 Explanation of the Interrupt Sources

INTERBUS-S inactive: A watchdog monitoring the INTERBUS-S activity and which can be parameterized via the SET-I register was executed.

SEND : Interrupt source for PCP communication. If this interrupt is present, the CPU can write a new communication word in the SUPI II. The SEND interrupt identifies a data or ID cycle end.

RECEIVE : Interrupt source for PCP communication. If this interrupt is present, the CPU can read a new communication word from the SUPI II. The RECEIVE interrupt identifies the end of a valid data cycle with the IDLE bit = 1.

INTERBUS-S reset : Due to a fatal error, this INTERBUS-S station has been set to the reset state.

INTERBUS-S cycle counter : An 8-bit counter loaded via the register, with the rel. address 8 and value n, counted n- valid data cycles. Before the interrupt occurs, the current counter value can be read via the relative address 8.

Identification cycle : This interrupt indicates the end of an indentification cycle.

Valid data cycle : This interrupt indicates the end of a data cycle. Current IB-OUT data is present. This interrupt can also be used for synchronizing the CPU access to the SUPI II.

Invalid data cycle : After this interrupt event, data of the OUT bytes originates from the last valid data cycle, since the just finished data cycle has been detected invalid. The CPU may write the IN bytes nevertheless.

Check sequence : The check sequence within an INTERBUS-S cycle. The IN and OUT bytes may only be written or read for 65 µs.

6.4.8.2 Synchronization Options

In principle, there are two options for synchronizing the INTERBUS-S cycles:

1. Use of interrupts

When the interrupt-controlled synchronization is used, the "Data Cycle" interrupt occurs.

How to proceed :
The interrupt is enabled by writing 40hex to the interrupt-enable register with the relative address 4 (only once during initialization).

After each interrupt request (/IRQ becomes low), the interrupt event II register with the relative address 5 has to be read.
If the contents of this register is 02hex , current data can now be read out of the IB-OUT data registers.
If the contents of this register is 04hex, IB-OUT data originates from the last valid data cycle.

Independent of the contents of the interrupt event II register, the CPU can write to the IB-IN data registers after the interrupt request.
After reading the interrupt event II register, the contents are cleared automatically and the IRQ line becomes inactive.

Note: The register contents mentioned above are only valid when the "Data-Cycle" interrupt is enabled.

Time requirements:

After an interrupt request (/IRQ low), the CPU has the following time periods available for reading the IB-OUT data registers and the interrupt event-II register, as well as for writing the IB-IN data registers:

$$t = ((48 + n * 16) * t_{Bit}) - 26.67\ \mu s$$

with t_{Bit} : Length of an INTERBUS-S-bit (typ.: 3.3 µs)

n : Number of 16-bit data words in the entire network

t : Permissible access time of the CPU

Please observe that the minimum time t is only present when the INTERBUS-S network consists simply of the user's station.

Example : Implemented station: 2 words (32 bits). The input and output direction is to be used.

The worst case time amounts to

-> t = 237 µs

After an interrupt request, the CPU has a maximum of 237 µs to read the interrupt event II register and the IB-OUT data registers 0-3 as well as to write the IB-IN data registers 0-3.

2. Use of the polling bit

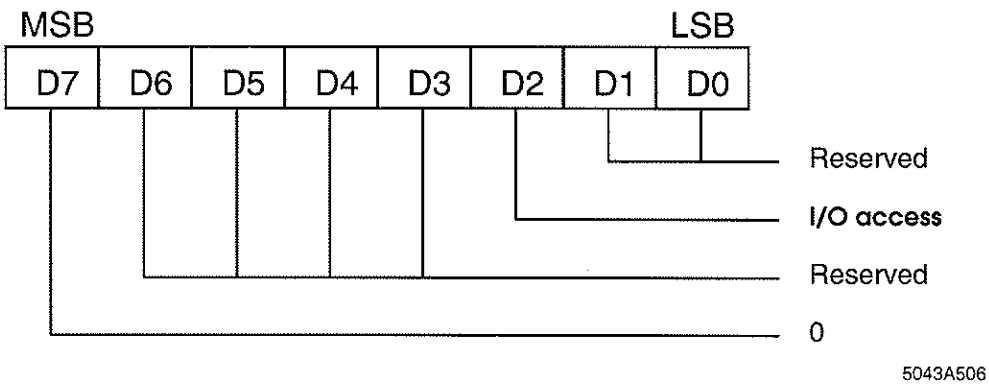
In the application, synchronization cannot be achieved via interrupts, so there is the possibility to poll the "I/O access" bit.

For this purpose, the IB state register with the relative address 7 must be read.

6.4.9 IB-State Register

Relative **read address : 7**

Assignment :



The bits marked 'reserved' have to be masked out.

If the I/O access polling bit has the value 1, the IB data register must not be accessed anymore.

If the I/O access bit is 0, access to the IB data registers may take place during the next 65 µs.
This time is independent of the station's data width and the INTERBUS-S configuration.

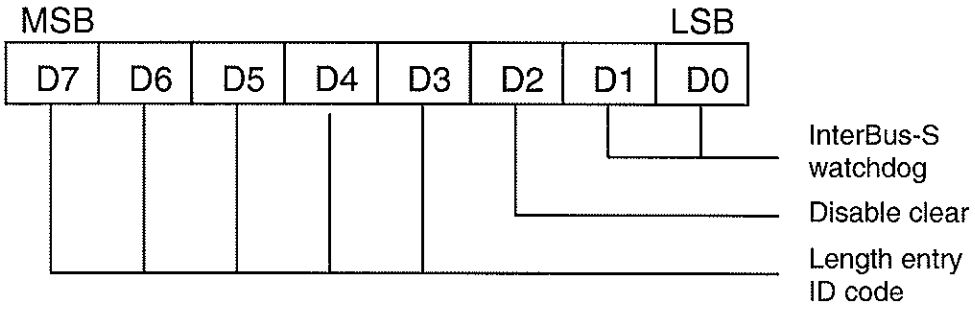
Therefore, synchronization via the polling bit places higher time demands on the CPU.

6.4.10 SET-I Register

Relative **write address : 5**

The SET-I register allows to paramterize the INTERBUS-S watchdog, and the length entry of the identification word can be preset.

Assignment:



Description of the INTERBUS-S watchdog

The INTERBUS-S watchdog monitors the physical data transfer on INTERBUS-S. The watchdog is reset with each incoming user data item.

This watchdog has two outputs :

a) BA output (Bus active)

This output, which is available as physical pin on the SUPI II chip, is used as the diagnostic output BA.
The off delay of BA is as long as the INTERBUS-S watchdog.

b) Interrupt source output 'INTERBUS-S inactive'

This interrupt is generated if the SUPI II has not detected any user data item until after the watchdog time elapsed.

The following table shows the parameterization options.

Table 6-12: INTERBUS-S watchdog in the SUPI II

D1	D0	Watchdog time/ms
0	0	640 (Default)
0	1	320
1	0	160
1	1	80

Disable Clear

For supporting the PCP communication it is required that the IB-IN bytes 0 and 1, which form the communication channel for PCP stations, are automatically cleared after they have been taken over by INTERBUS-S.

This clearing mechanism is enabled by default.

In order to use the two IB-IN bytes 0 and 1 for dedicated I/O applications, the clearing meachnism can be disabled with the 'Disable Clear' bit.

After this bit has been set, the data item written in the IB-IN bytes 0 and 1 is transferred in each data cycle.

Thus, the IN bytes 0 and 1 act in the same way as the IN bytes 2-3 and 10 -13.

	Disable Clear Bit
PCP station	0
I/O station	1

Length entry of the identification code

The length entry determines the data register width of an INTERBUS-S station (see also Chapter "ID Code").
By default, this length entry is wired via the SUPI II pins ID12 - ID 8 by hardware.

The SUPI II offers the possibility of setting the length entry of the identification code in the SET-I register by means of software.
This allows to adapt the data width to the application without changing the hardware.

Note : The ID length bit in the SET-II register is to be set to 1 for the length entry to become valid!

Mapping of the SET-II register on the length entry in the ID code.

SET-II register	D7	D6	D5	D4	D3
ID code	ID12	ID11	ID10	ID9	ID8

The meaning of the ID length bits ID12 - ID 8 can be taken from the following table.

Table 6-13: Encoding of the data width in the SET-I register

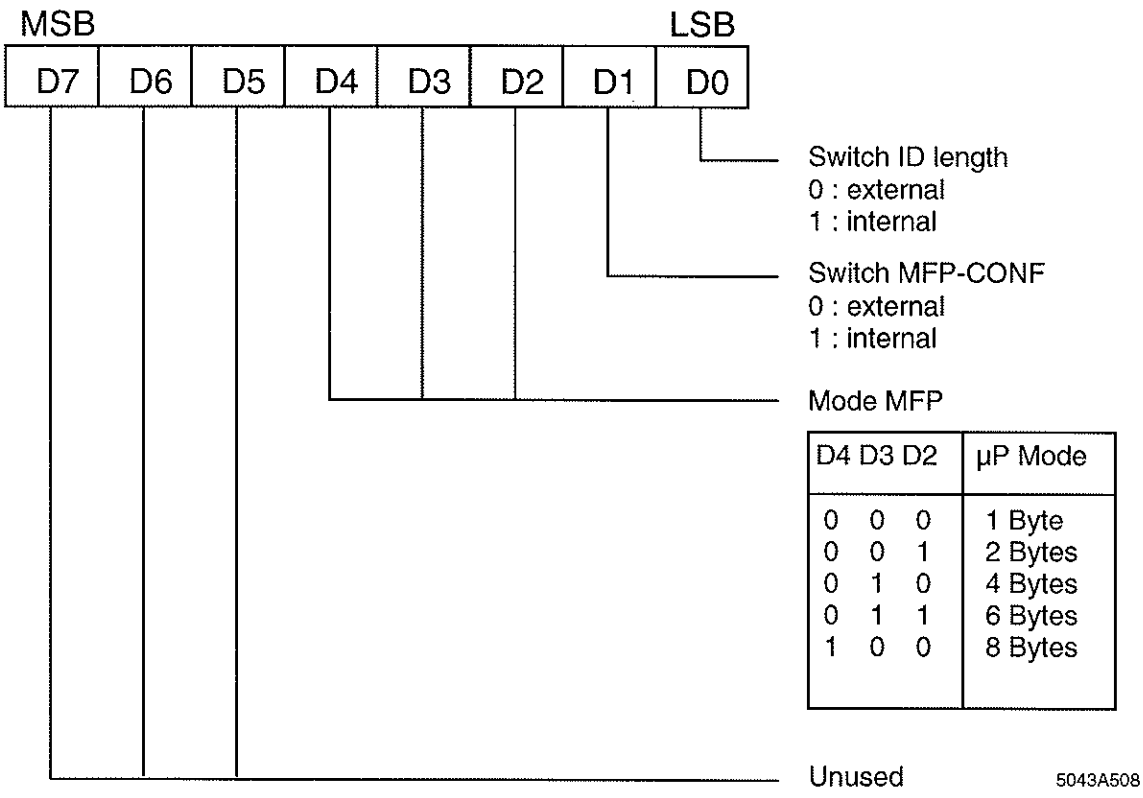
ID12	ID11	ID10	ID9	ID8	Data width
0	0	0	0	0	0 Words
0	0	0	0	1	1 Word
0	0	0	1	0	2 Words
0	0	0	1	1	3 Words
0	0	1	0	0	4 Words
0	0	1	0	1	5 Words
0	0	1	1	0	8 Words
0	0	1	1	1	9 Words
0	1	0	0	0	1 Nibble **
0	1	0	0	1	1 Byte **
0	1	0	1	0	3 Nibbles **
0	1	0	1	1	3 Bytes **
0	1	1	0	0	5 Nibbles **
0	1	1	0	1	5 Bytes **
0	1	1	1	0	6 Words *
0	1	1	1	1	7 Words *
1	0	0	1	0	16 Words *
1	0	0	1	1	24 Words *
1	0	1	0	0	32 Words *
1	0	1	0	1	10 words *
1	0	1	1	0	12 Words *
1	0	1	1	1	14 Words *

* This data width will only be supported as of firmware version 3.20 by the controller board and as of version 2.0 by the PC AT board.
** This data width is currently not supported.

6.4.11 SET-II Register

Relative **write address : 6**

Assignment:



D4	D3	D2	µP Mode
0	0	0	1 Byte
0	0	1	2 Bytes
0	1	0	4 Bytes
0	1	1	6 Bytes
1	0	0	8 Bytes

Description :

Switch ID length : This bit allows to separate the hardware connections of pins ID12 - ID8 and to reroute them to bits D7 - D3 of the SET-I register.

Switch MFP-CONF: MFP-CONF allows to separate the hardware connections of pins C3 - C0 and to map them onto the table with the bits D4 - D2 of the SET-II registers.

Mode MFP: In the µP modes of operation the SUPI II register width can be set using this table.

6.4.11.1 Example of an Application

The following example is to show how to proceed when you are using the ID length and MFP mode bits :

Example: Depending on the degree of extension, an application requires data widths of 16 to 32 bits.
The changeover is to be done without changing the hardware, i.e. by the CPU.

Solution: The SUPI II is set to the mode "µP interface 2 bytes" using the hardware pins C3-C0 and to the data width of one word with pins ID12 - ID 8. If the application requires a data width of 32 bits, the following write commands have to be executed:

1) Writing 14hex in the SET-I register
2) Writing 0Bhex in the SET-II register

Please observe that these changeovers commands are only to be executed during the initialization phase and not during operation.

7. Register Expansion

If the data width of the SUPI II is to be widened or supplemented, this can be done, indenpendent of the selected mode of operation, using external shift registers.

The SUPI II has two shift register data outputs. The **ToExR1** output lies before and the **ToExR2** output after the SUPI II-internal shift registers.

The **FromExR** input is provided for the feedback of the shift register data.

The **/CLKExR** signal is to be used as clock for the external registers.

The active low **/LaInD** signal is used as a transfer signal from the application to the shift registers and the active high **LaOuD** signal is used as latch signal from the shift registers to the application.

The active low **/ResReg** signal is available for resetting the external memory registers after an INTERBUS-S reset.

There is a number of combination options for a register expansion.

Example.:

a) No register expansion
Pins ToExR2 and FromExR have to be connected with each other. The internal SUPI II registers are used only.

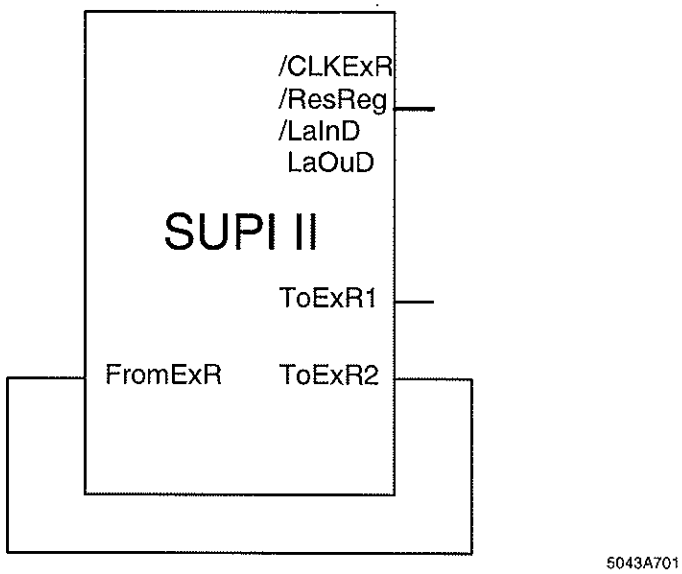


Figure 7-1: No register expansion

b) Expansion of the SUPI II-internal INTERBUS-S data registers:
The external shift registers are to be connected to the output ToExR2 and to lead back to the input FromExR. Both, IN and OUT registers are possible.

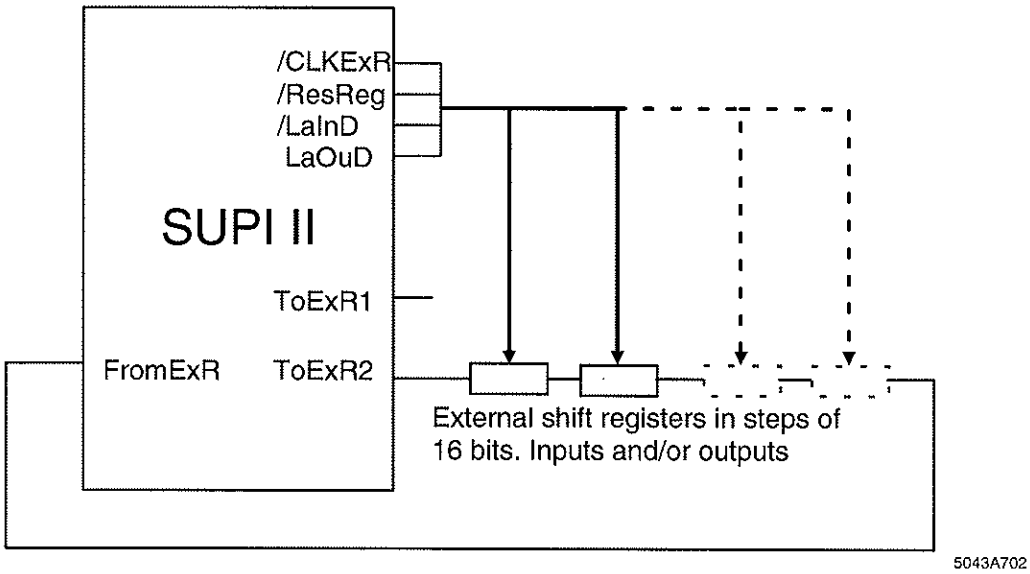


Figure 7-2: Expansion of the internal SUPI II registers by means of register expansion

c) Implementation of a 16-bit station with 16 inputs and 16 outputs, using the SUPI II as a 16-bit output:
In this case, a 16-bit shift register (loadable asynchronously and in parallel) is to be connected between pins ToExR1 and FromExR.

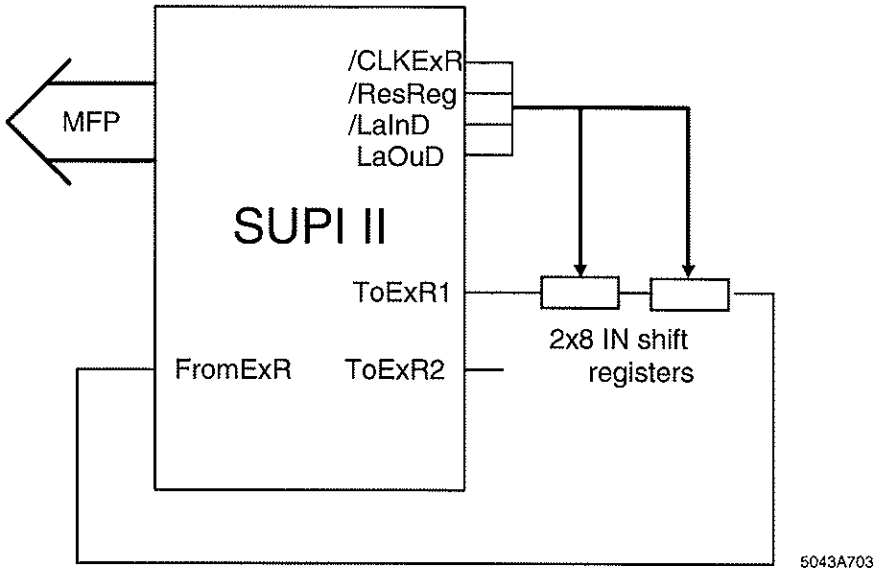


Figure 7-3: 16-bit I/O station with 2x8 bit IN register expansion

d) Implementation of an I/O station with 32-bit inputs and 16-bit outputs
There are different ways of assigning an address. The internal registers of the SUPI II can be used as inputs, outputs or not at all. In addition it is also possible to assign different data widths to such a station. The following figures show the different ways.

d1)48-bit station with 16 OUT and 32 IN addresses. The internal SUPI II registers have been used as outputs and extended by 4x8-bit shift registers with inputs.

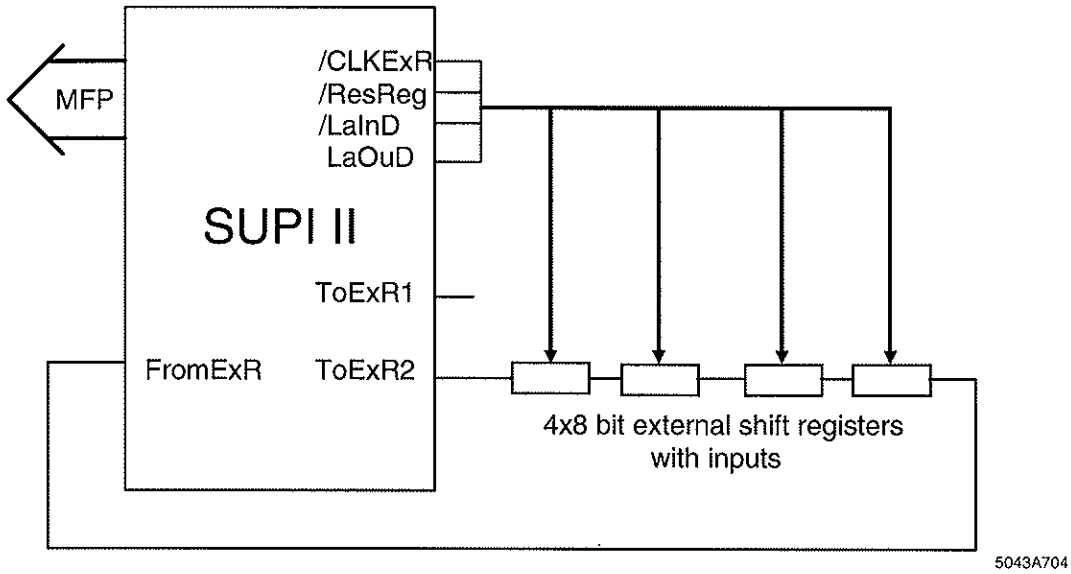


Figure 7-4: 48-bit I/O station with 4x8-bit IN register expansion

d2)48-bit station with 16 OUT and 32 IN addresses. The internal SUPI II registers have been used as inputs and have been extended by 4x8-bit shift registers with inputs and outputs.

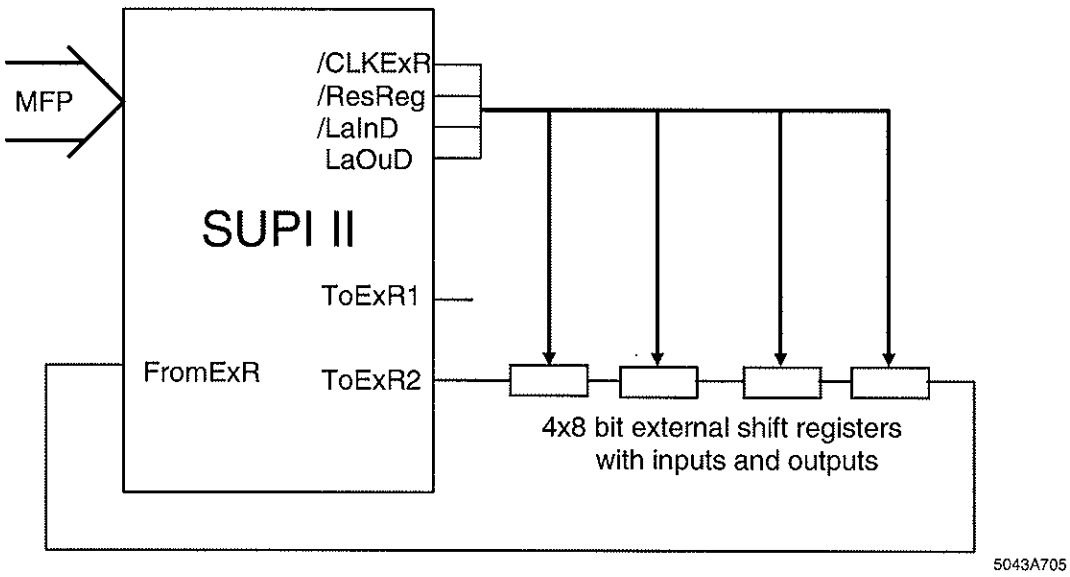


Figure 7-5: 48-bit I/O station with 2x8-bit IN and 2x8-bit OUT register expansion

d3)32-bit station with 16 OUT and 32 IN addresses. The internal SUPI II registers have been used as outputs. Parallel to this, 4x8-bit shift register with inputs have been looped in between the pins ToExR1 and FromExR.

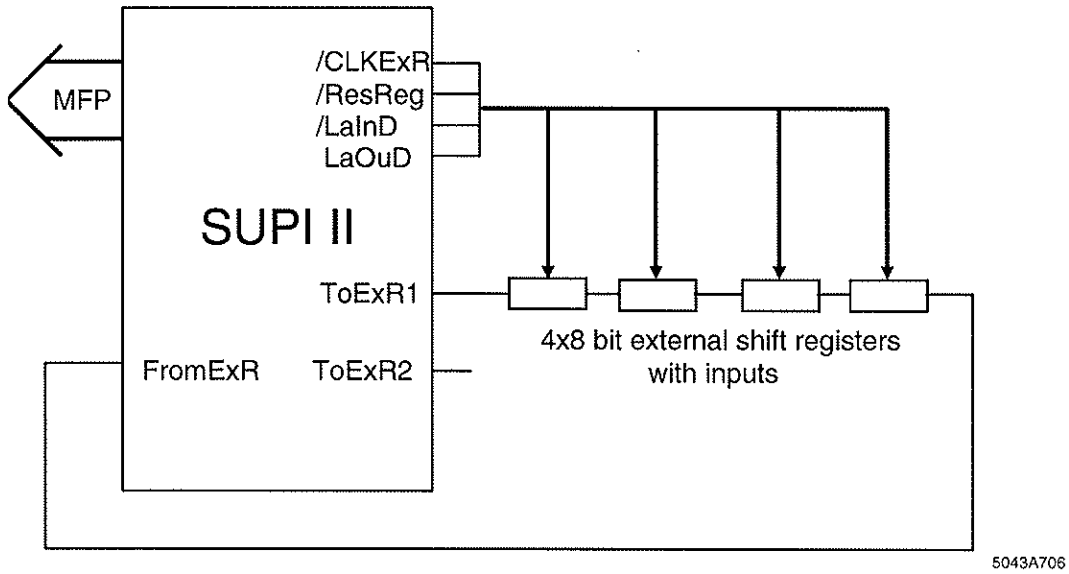


Figure 7-6: 32-bit I/O station with 4x8-bit IN register expansion

d4)32-bit station with 16 OUT and 32 IN addresses. The internal SUPI II registers are used as inputs and are extended by 2x8-Bit IN registers.
Parallel to this, 2x8-bit shift registers with outputs are connected with ToExR1.

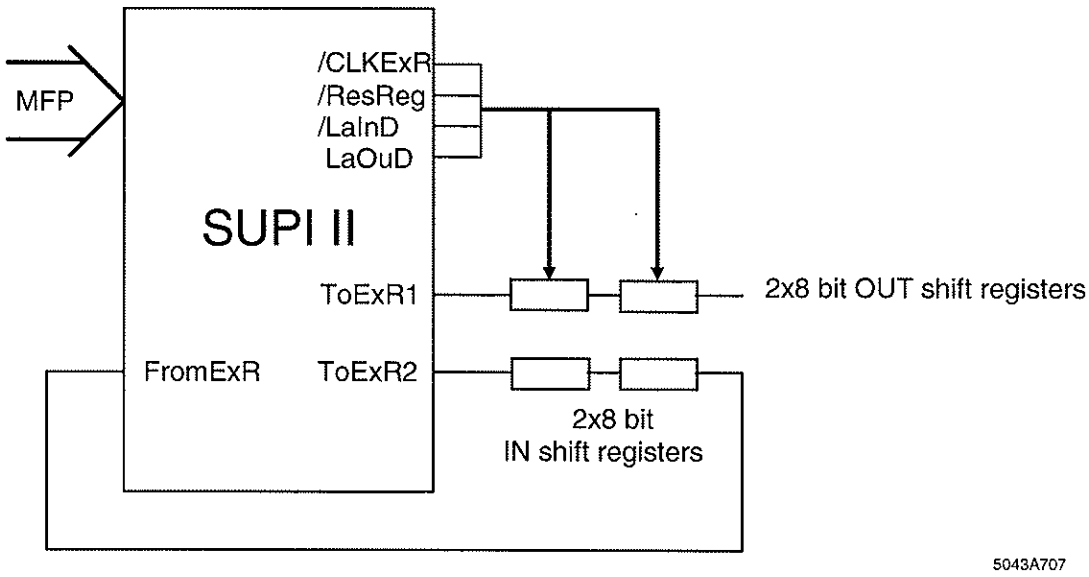
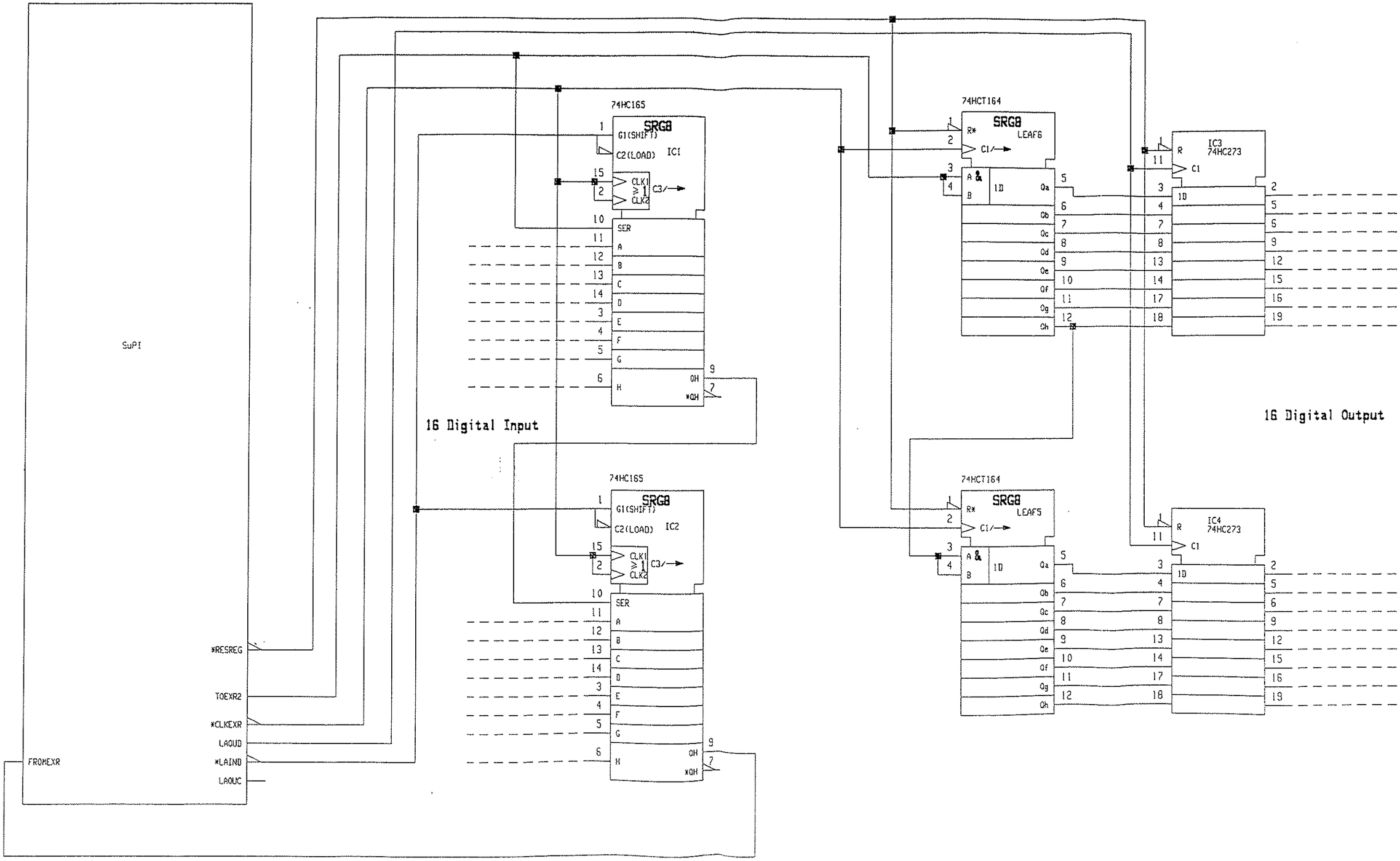


Figure 7-7: 32-bit I/O station with 2x8-bit IN and 2x8-bit OUT register expansion

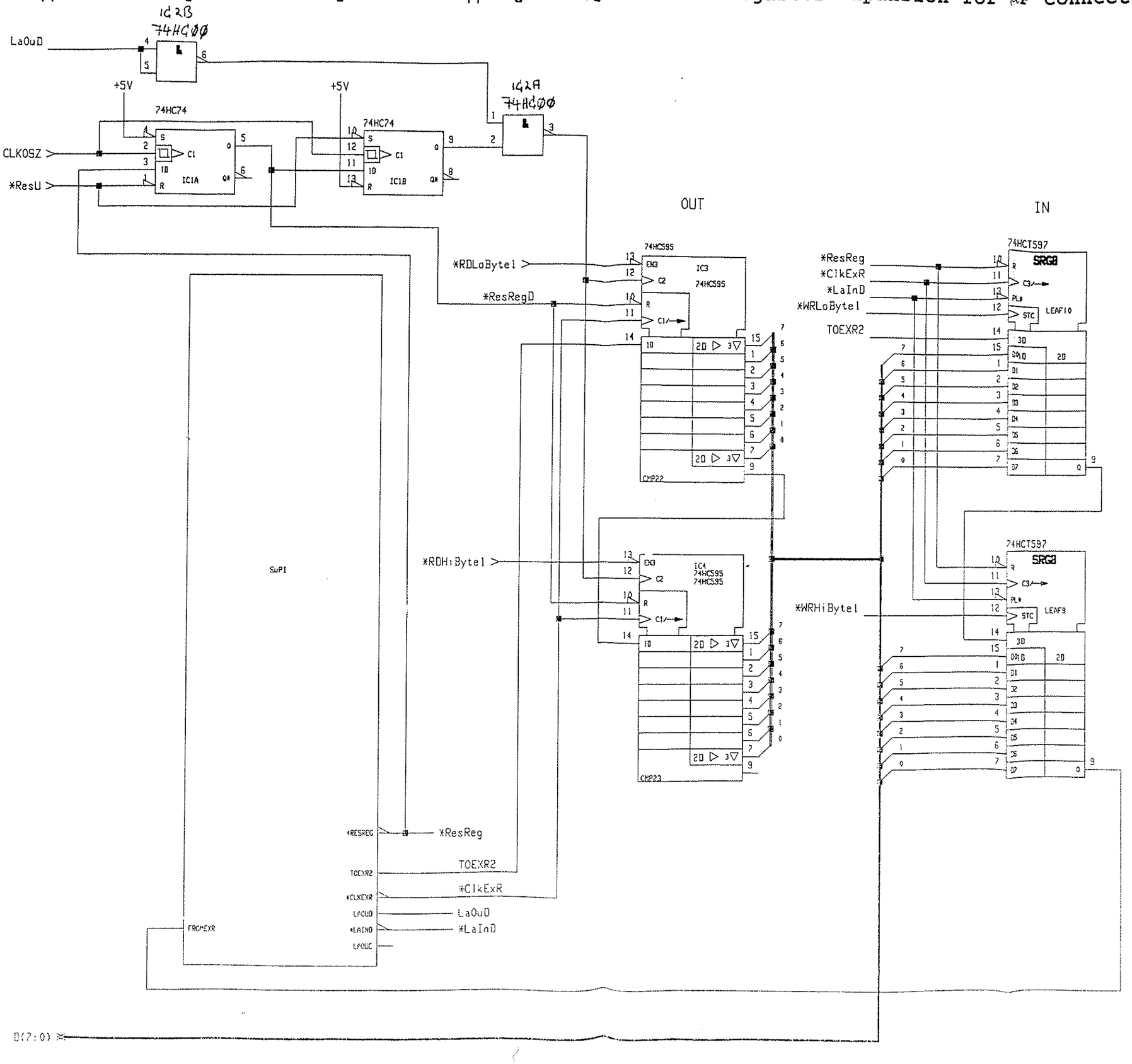
The following two applications show a register expansion by 16 bits for dedicated I/O data or microprocessor access.

Applikation : Registererweiterung fuer I/O-Daten

(Application : Register expansion for I/O data)



Applikation : Registererweiterung fuer uP-Ankopplung (Application: Register expansion for µP connection)



8. Diagnostic Inputs/Outputs

The SUPI II protocol chip has different diagnostic inputs and outputs, which simplify the location of error sources within the INTERBUS-S network.
The inputs and outputs to be used for diagnostics depend on the physical location of the station within the INTERBUS-S network and its functionality.

Remote bus station:

Table 8-1: Diagnostic inputs/outputs of a remote bus station

Mode	RC	BA	TR	Module error	RBDA	LBDa	Conf
Bus terminal mod.	X	X			X	X	X
16-bit output	X	X		X	X		
16-bit input	X	X		X	X		
8-bit I/O	X	X		X	X		
µP	X	X	X	X	X		

Local bus station:

Table 8-2: Diagnostic inputs/outputs of a local bus station

Mode	TR	Module error
16-bit output		X
16-bit input		X
8-bit I/O		X
µP	X	X

Explanation of the diagnostic inputs and outputs:

RC

The green RC (**R**emote bus **C**heck) diagnostic LED is connected to the CMOS output /ResReg of the SUPI II chip.
RC has the job of monitoring the remote input cable.
If the cable connection is good and the IB master is not reset, then the RC is active.
The RC LED becomes inactive in the event of an INTERBUS-S reset or a power-up reset.

BA

The green BA (**B**us **A**ctive) LED at the output signals an INTERBUS-S transmission. The output has an off delay of the duration of the preset IB timeout (default: 640 ms).

TR

the green TR (**T**ransmit/**R**eceive) diagnostic LED becomes active when PCP communication is being carried out via INTERBUS-S. It is connected to the active high SUPI II LBDA/TR pin in the µP modes. An external off delay is provided for this output, in order to guarantee a visible indication on the LED. The output pulse has a minimum length of 12 µs.

Module error at the input/output

Input:

The active low input /StatErr is used, for example, to report a module error (e.g., pheripheral voltage not applied) to the INTERBUS-S master.
Applying a low level to this input causes a module error.

If /StatErr is not used, it has to be statically connected to Vdd.

Acknowledge output:

The /ModAck output can be used as an acknowledge output for a set module error. In the master, this error is acknowledged with the following commands:

64hex Quit Module Error or
65hex Quit Module Error All.

This output will then be active for exactly 4 bit times (13.2 µs at 500 kBaud).

CONF

Only in bus terminal applications is the CONF signal input used to request a reconfiguration for the INTERBUS-S network.

If this input is not used, it has to be statically connected to Vss.

RBDA

The active high RBDA pin indicates that the outgoing remote bus is disabled (**R**emote **b**us **d**isa**b**le) This diagnostic option is only relevant for remote bus stations and is indicated by a red LED.

LBDA

In bus terminal modules, the active high LBDA/TR pin indicates that the local bus is disabled (**L**ocal **b**us **d**isa**b**le) and is also indicated with a red LED.

9 Electrical Data

Table 9-1: Electrical data of the SUPI II chip

Electrical data	Value
-- General data --	
Voltage supply V_{dd}	4.5 V ... 5.5 V
Input voltages	-0.5V ... V_{dd}+0.5V
Current consumption *)	≈20 mA
Temperature range	-40 °C ... +85 °C (industrial)
-- CMOS inputs --	
CMOS input voltage high	3.5V ... V_{dd}+0.5V
CMOS input voltage low	-0.5V ... 1.5V
-- Schmitt Trigger inputs --	
Schmitt Trigger inputs positive going threshold	2.4V ... 3.8V
Schmitt Trigger inputs negative going threshold	1.1V ... 2.4V
-- CMOS outputs B2 --	
CMOS output voltage high	3.7V min
CMOS output voltage low	0.4V max
CMOS output current	2 mA
-- Driver outputs BD, B12 --	
Driver output voltage high	each 5 mA -> Vdd -0.2V
Driver output voltage low	each 5 mA -> Vdd +0.1V
Driver output current	4/12 mA

*) All inputs are static, outputs are not connected, oscillator operates with 16 MHz.

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